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303H Fall 2013

Homework 7 – due Tu 10/29/13

Use 4007 CMOS transistors with bias at VDD (= a 1) with respect to ground (= a 0) and run Spice for the following problems.

1. 50 points (CMOS NANDs).
   a) A two input NAND gate (Fig. 13.32, p. 1114) feeding an inverter. Consider the four possible binary inputs and compare (a table would be useful) the four values of delay between the NAND inputs and the inverter output. (use VDD/2 as delay calculation points).
   b) Repeat part a) using three NAND gates with the same inputs feeding the one inverter and compare delays with those of part a).

2. 50 points (Pass transistor logic)
   For the pass transistor logic (PTL) circuits of Fig. 14.7, p. 1154 with an output inverter in (b) as in (a), consider C as the input capacitance of the output inverter (so no need to add it in a schematic) and consider the four binary combinations for A and B.
   a) Plot the signals A, B, Y and voltage output of the right hand inverters using the single NMOS pass transistor of Fig. 14.6 (a) with the bulk tied to ground.
   b) Repeat part a) using the CMOS pass transistors of Fig. 14.6(b) with the PMOS bulk tied to VDD.
   c) Compare the different Y values and explain any differences between the results for Fig. 14.7 (a) versus (b).
   d) Tie the bulk in part a) to the A terminal and repeat a). Discuss the results obtained.