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303H Fall 2013

Homework 5 – due Tu 10/15/13

1. 50 points (CMOS inverter)

Use a CMOS 4007 pair to construct an inverter. Use one battery of V_{DD}=5V, for use of the inverter in binary circuits where a 1 is represented by V_{DD} and 0 by ground=0V. (All voltages are measured with respect to ground, the input is at the common gate and the output is at the common drain; the bulks are tied to the sources). Submit the mentioned plots.

a) For an open circuit load do a DC run in Spice plotting Vout versus Vin for $0 \leq Vin \leq V_{DD}$. Determine the Vout value for Vin=V_{DD}/2; comment on any deviation from Vout=V_{DD}/2.

b) Make three plots on one page (use PSpice "add a plot") one for Vout vs Vin, a second one for the NMOS VDS and VGS-VTO vs Vin, and the third one for the PMOS of VSD and VSG-|VTO| vs Vin. From these determine at what Vin the CMOS transistors are in the saturation and when in the Ohmic (=triode) regions.

c) Repeat part a) but change the battery to V_{DD}=10V.

2. 50 points (inverter transient response)

For the above inverter with V_{DD}=5V

a) Run a transient response for Vin(t) a step-like function rising from 0 to V_{DD} with rise time of 2pS, plotting Vout(t) and Vin(t) in the same plot. Repeat for Vin(t) a step-like function falling from V_{DD} to 0 with fall time of 2pS. Compare the responses commenting upon delay through the inverter. (Run the curves for sufficient time to go to at least 90% of the final output voltage of 0 or V_{DD}).

b) Repeat part a) when the output is loaded with a 10nFd capacitor (from output to ground), assuming the capacitor initial condition (IC) at t=0 is the complement of the input voltage at t=0. Compare the rising and falling responses and also compare with those of part a).

c) Repeat part a) when V_{DD}=10V.