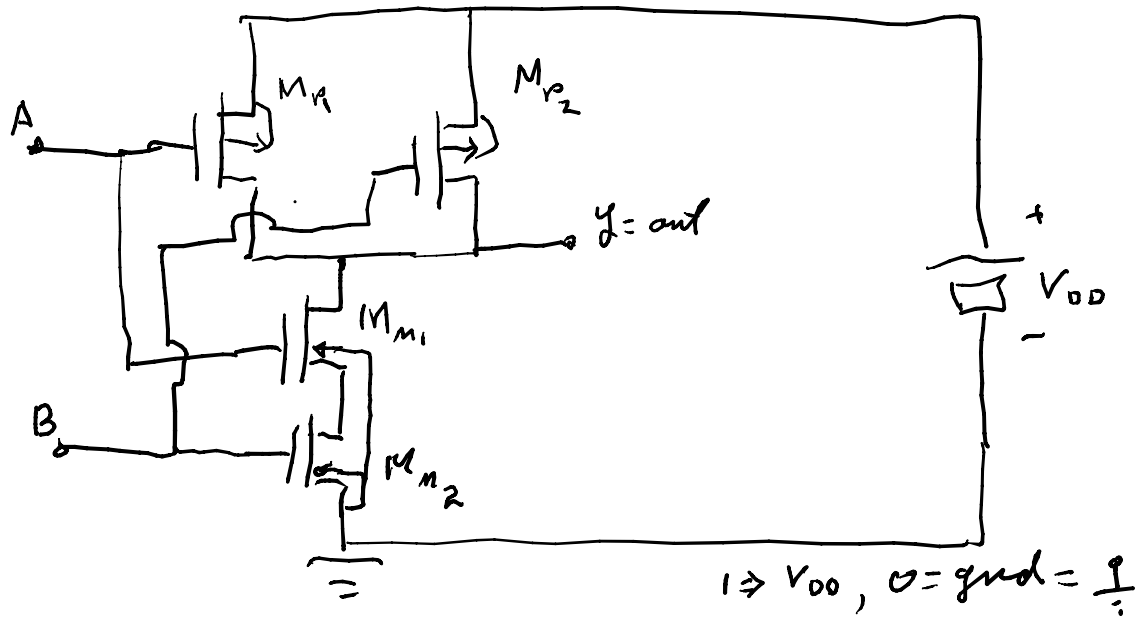
EE 303H
10/24/13

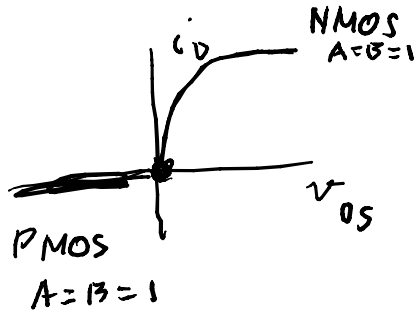
Note Title 10/24/2013

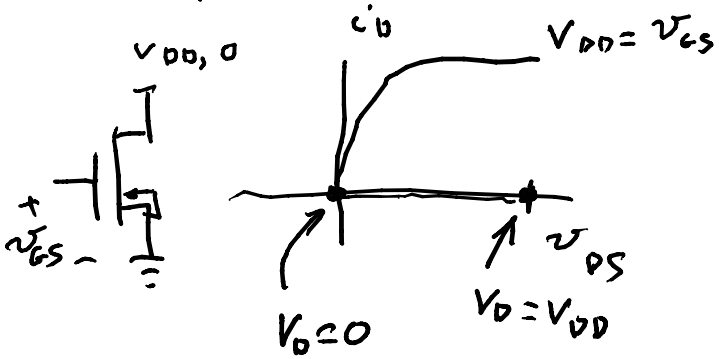
P. 1114 NAND CMOS



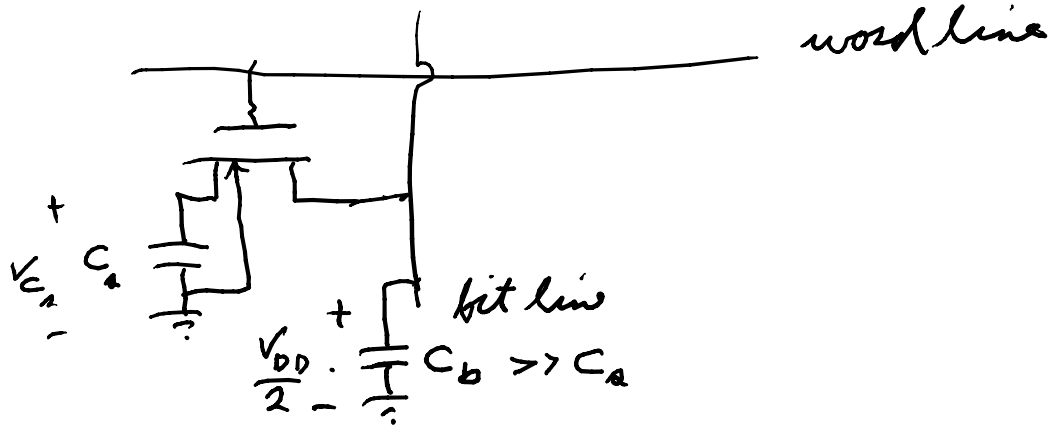
"Table"

A	B	y
1	1	0
1	0	1
0	1	1
0	0	1



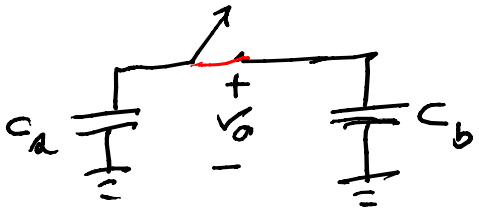


Dynamic RAM p. 1224



if $V_{C_A} = V_{DD}$ $V_{CB} \approx V_{DD}/2$ if address transitor
$\Rightarrow$ a 1 stored

$V_{C_A} = 0$
$\Rightarrow$ 0 stored



Q = charge before switch

$$C_a V_{CA} + C_b \cdot \frac{V_{DD}}{2} = (C_a + C_b) \cdot V_0$$

if $V_{C_A} = 1 \Rightarrow$ $C_a V_{DD} + C_b \cdot \frac{V_{DD}}{2} = (C_a + C_b)\left(\frac{V_{DD}}{2} + \Delta V\right)$ $C_b >> C_a$

$$C_a V_{DD} = C_a \frac{V_{DD}}{2} + C_a \Delta V + C_b \Delta V, \Rightarrow C_a\left(\frac{V_{DD}}{2}\right) = (C_a + C_b)\Delta V$$

$$\Delta V = \frac{C_a V_{DD}/2}{C_a + C_b}, \quad \Delta V \simeq \frac{C_a}{C_b} \cdot V_{DD}/2$$

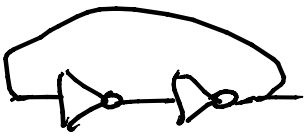
if $V_{C_a} = 0$ $C_b \frac{V_{DD}}{2} = (C_a + C_b)\left(\frac{V_{DD}}{2} - \Delta V\right)$

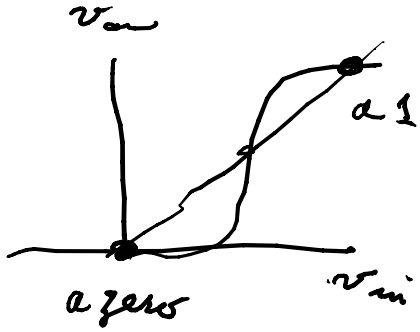
$$0 = C_a \frac{V_{DD}}{2} - C_a \Delta V - C_b \Delta V \quad \Rightarrow \Delta V = \frac{C_a}{C_B} V_{DD}/2$$

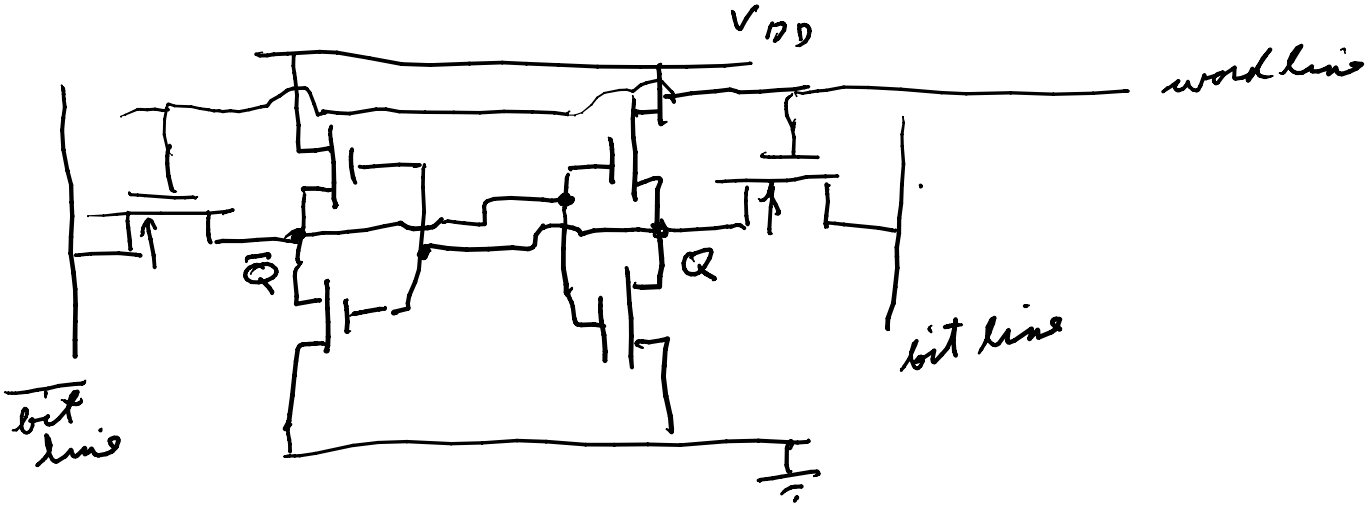
$$\therefore V_{C_b} = \frac{V_{DD}}{2} - \frac{C_a}{C_b}\frac{V_{DD}}{2} = \left(1 - \frac{C_a}{C_b}\right)\frac{V_{DD}}{2} < V_{DD}/2$$

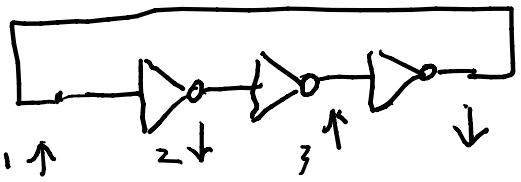
to restore replace V_{DD} by $V_{DD} + \Delta V$ when finish measuring a 1; also need to refreshing

SRAM



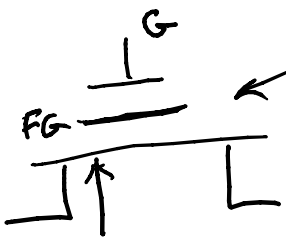




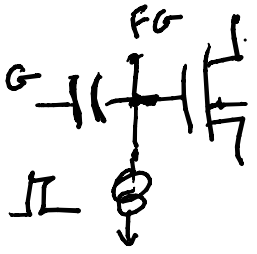


ring oscillator
P. 1239

floating gate



model



D flip flop