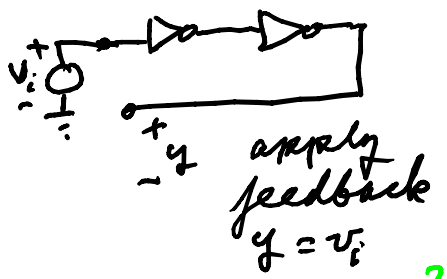
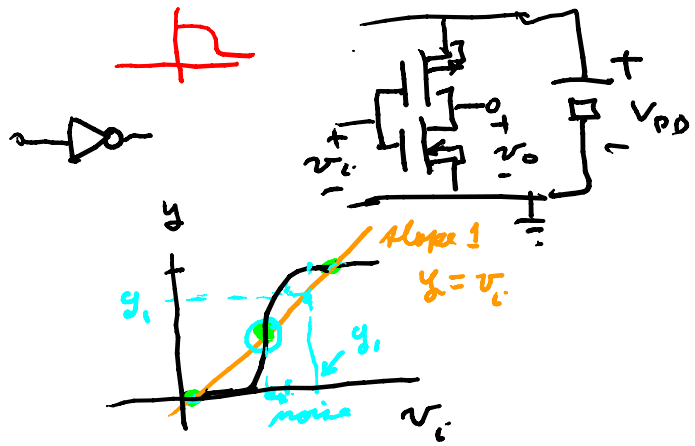
EE 303
10/16/12

Note Title 10/10/2012

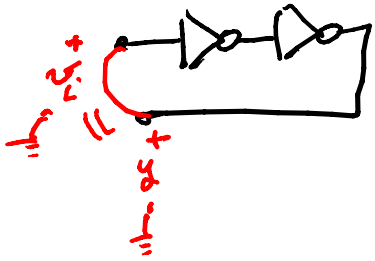
latch

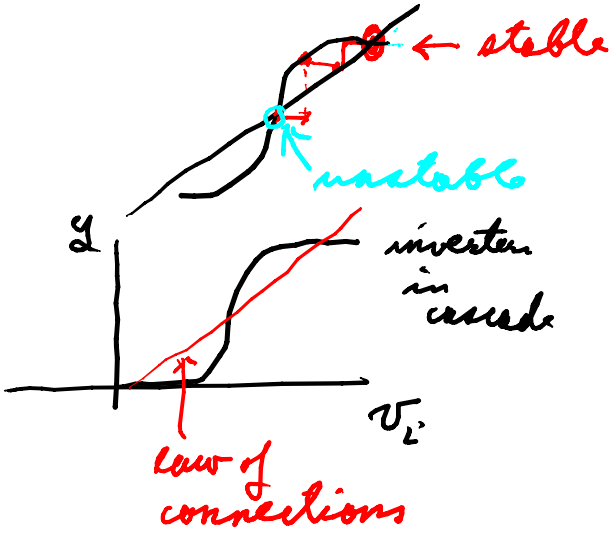
P. 1206
F 15.3





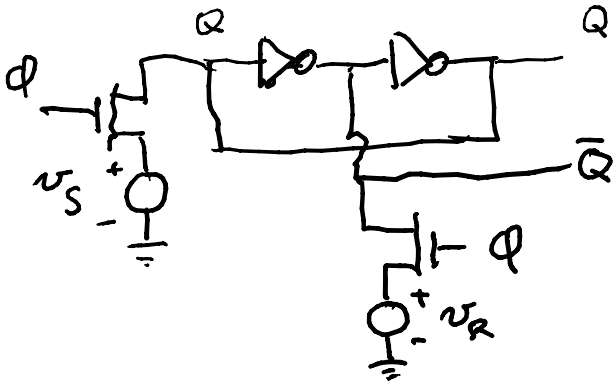
3 bias points 2 unstable





clocked SR

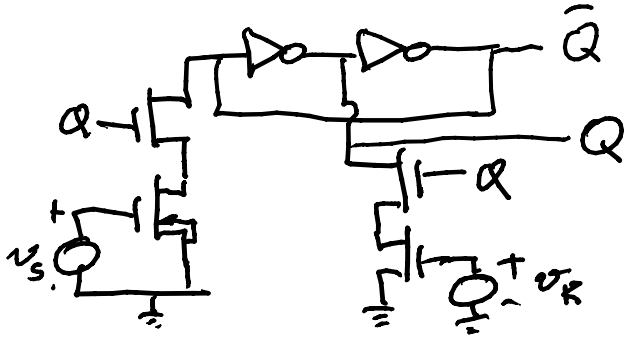
P. 1212
F 15.7



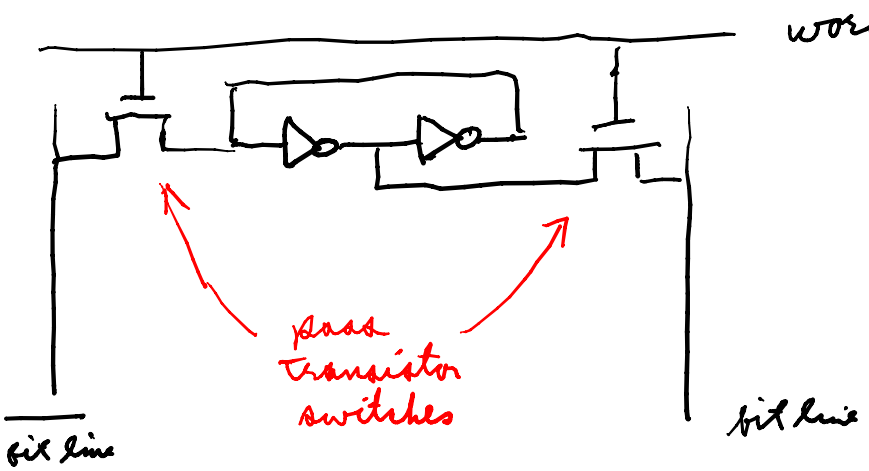
ϕ = clock square wave 0 & V_{DD} amplitude on pass transistor switches

also on

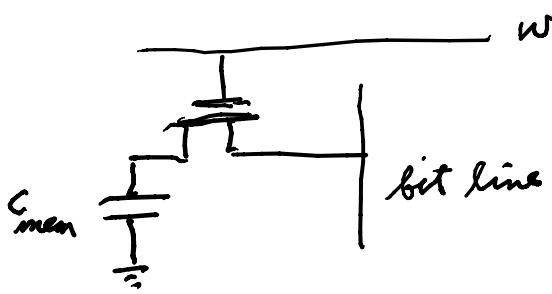
P. 1207
F 15.4



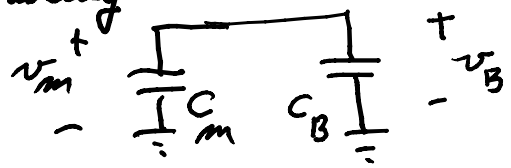
SRAM
P. 1218
F 15.12



DRAM
P. 1225
F 15.18



For reading



for $t = 0_-$
pass transistor = open
$v_B = V_{DD}/2$
if a 1 is in memory $v_m = V_{DD}$

at $t = 0_+$ switch closed

charge total $t = 0_-$ = same charge $t = 0_+$

$$C_m v_{m_{0_-}} + C_B v_{B_{0_-}} = (C_m + C_B) v_{B_{0_+}} \quad ; \quad v_{B_{0_+}} = V_{DD} + \Delta V_B$$

normally $C_m < C_B \approx 10 C_m$

$$C_m \cdot V_{DD} + C_B \frac{V_{DD}}{2} = (C_m + C_B) \cdot v_{B_{0_+}}$$

$$= (C_m + C_B)\left(\frac{V_{DD}}{2} + \Delta V_B\right)$$

$$(C_m + C_B)\frac{V_{DD}}{2} + C_m \frac{V_{DD}}{2} = (C_m + C_B)\frac{V_{DD}}{2} + (C_m + C_B)\Delta V_B$$

$$\Delta V_B = \frac{+C_m}{C_m + C_B} \cdot \frac{V_{DD}}{2} \approx +\frac{1}{11} \cdot \frac{V_{DD}}{2}$$

for a 1 stored

Physically; if C_{mem} has a 1 it raises v_B when connected & if a 0 it lowers v_B. So sense if v_B goes up or down to detect what is in memory

for a 0, $v_{m_0^-} = 0 \Rightarrow \frac{C_B V_{DD}}{2} = (C_m + C_B)\left(\frac{V_{DD}}{2} + \Delta V_B\right)$

$$0 \cdot \frac{C_B V_{DD}}{2} - C_m \frac{V_{DD}}{2} = \Delta V_B (C_m + C_B)$$

$$\frac{-C_m}{C_B + C_m} \cdot \frac{V_{DD}}{2} = \Delta V_B$$

if $C_B = 10 C_m \Rightarrow -\frac{1}{11}\frac{V_{DD}}{2} = \Delta V_B$ if a 0 is stored

op-amp

VCVS

high voltage gain

μA 741 op-amp