File G/courses/F2012/303/303F12hmrk5.doc RWN 10/05-15/12

303 Fall 2012

Homework 6 – due 10/16/12

1. 50 points (OTA)
   a) Design a DVCCS using 4007 CMOS transistors with a tail current of I_T = 1mA such that Iout =I1 – I2 (delete = I_T) for large positive vin. Calculate the Gm value at the vin=vid=0. Use Vdd=-Vss=5V.
   b) Do a DC run of Spice to give the Iout versus vin=vid curves and check the value of Gm obtained.
   c) Run a frequency response of Iout versus v1 with v2=0 from 10 Hz to 100MHz.
   d) Rerun the DC curves to obtain the curves of b) and on the same graph compare with the formula Iout=I_T*tanh(vin/(2V_T)) [you can use a Gvalue for this]

2. 50 points (NAND Gate)
   Use the 4007 CMOS transistors to make a NAND gate (as in Figure 13.32 of the text) using Vdd=5V.
   a) Run a Spice transient response with the voltages for A and B coming from pulses which switch on a milli-second scale between 0 and Vdd to cover all four bit possibilities.
   b) Repeat by switching bits on a nano-second scale and comment on the results.