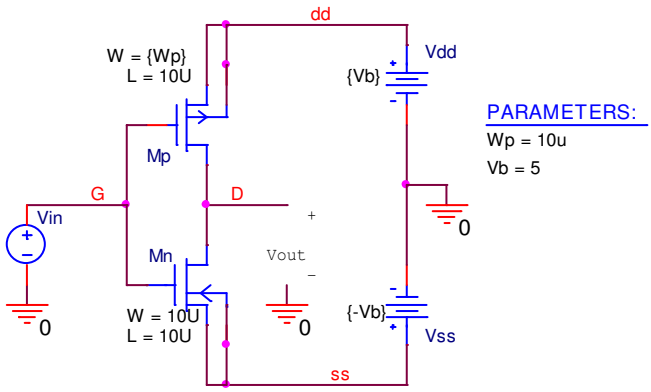
File G/courses/F2012/303/303F12hmrk5.doc RWN 09/28/12

303 Fall 2012

Homework 5 – due 10/09/12

1. 50 points (CMOS inverter)
   For the following CMOS inverter use mnmosis & mpmosis transistors
   a) Analytically choose the PMOS width, Wp, so that 0 input gives 0 output. Adjust via DC runs of Vout versus Vin, from Vin =Vss = -5 to Vin=Vdd=+5, in Spice using parametric runs on Wp.
   b) For the adjusted transistors choose the bias parameter, Vb, from +2 to +5 in 1 V steps for Vdd and –Vss, and do DC runs over Vin from -2 to +2 and check the value of output for input of 0.



2. 50 points (inverter response)
   For the inverter of problem 1, assume v_{in} is a small signal with the circuit Q point at $V_{IN}=V_{OUT}=0$.
   a) Find the low frequency gm (=y21) and go (=y22) for the 2-port with the input-ground as port 1 and output-ground as port 2.
   b) At port 2 load in a capacitor and analytically find the transfer function of $v_{out}/v_{in}(s)$ in terms of generic gm, go and C.
   c) Analyticallu give the unit step response.
   d) Use a load capacitance of 20nFd and vin(t) a pulse of 0.2V and width 1mS; run Spice for 10mS. Submit the results and comment upon them.

   The input can be chosen as the following: