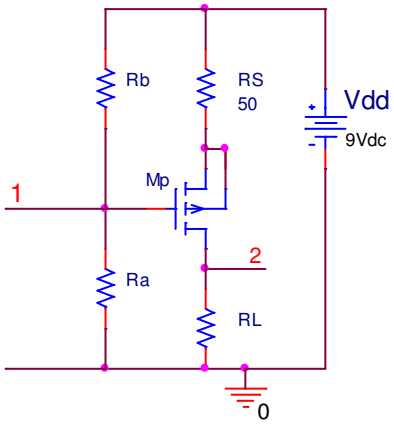
File G/courses/F2012/303/303F12hmrk4.doc RWN 09/23/12

303 Fall 2012

Homework 4 – due 10/02/12

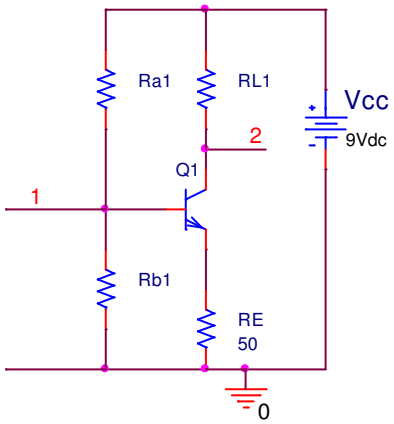
1. 50 points (PMOS biasing)

Bias the PMOS 4007 in the following circuit to have a Q point at VGS=-3V, VDS=-5V. For this assume an RS=50Ω, Vdd=9V, and one of Ra or Rb of 10MegΩ. Check using Spice. Give the small signal low frequency voltage gain, $Av=V_{20}/V_{10}$.



2. 50 points (BJT npn amplifier)

Bias the 2N3904 in the following circuit to have a Q point at IC=3mA, VCE=5V. For this assume an RE=50Ω, Vdd=9V, and one of Ra or Rb to be the maximum possible value within a power of 10 of 10MegΩ. Check using Spice. Give the small signal low frequency voltage gain, $Av=V_{20}/V_{10}$.



2. 25 points (frequency response)

Insert a 50uFd coupling capacitor in series with node 1 of the circuit of problem 2 and on its left a VAC and in Spice run a frequency response plotting V2 from 10Hz to 1GHz.