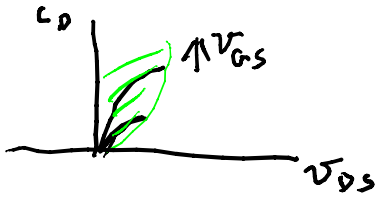
EE303H
09/27/11

Note Title 9/27/2011

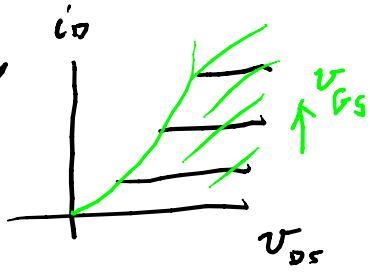
3 regions of operation of an MOS transistor

NMOS cutoff, only sub threshold current, $0 \le v_{GS} \le V_{th}$ " V_{TO} if $v_{BS}=0$

ohmic = triode, somewhat linear $0 \le v_{DS} \le v_{GS} - V_{th}$



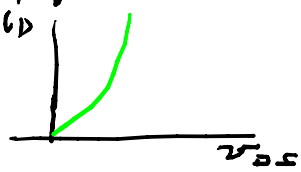
saturation, almost constant current square law

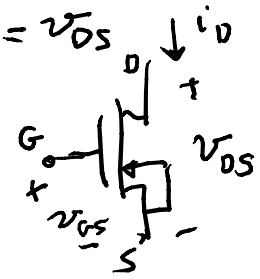


$$i_D = \frac{KP}{2}\cdot\frac{W}{L}\cdot\begin{cases} 0 & 0 \le v_{GS} \le V_{th} \text{ cutoff} \\ (2(v_{GS}-V_{th})v_{DS} - v_{DS}^2) & 0 \le v_{DS} \le v_{GS}-V_{th} \text{ ohmic} \\ (v_{GS}-V_{th})^2 & 0 \le v_{GS}-V_{th} \le v_{DS} \text{ saturation} \end{cases}$$

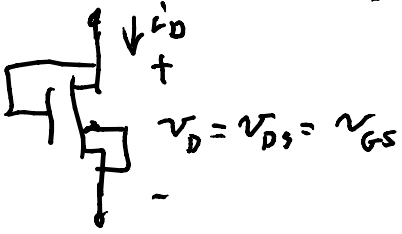
at transition between on regions $v_{GS}-V_{th} = v_{DS}$

$i_{D_{sat}} = \frac{KP}{2}\frac{W}{L}\cdot v_{DS}^2$

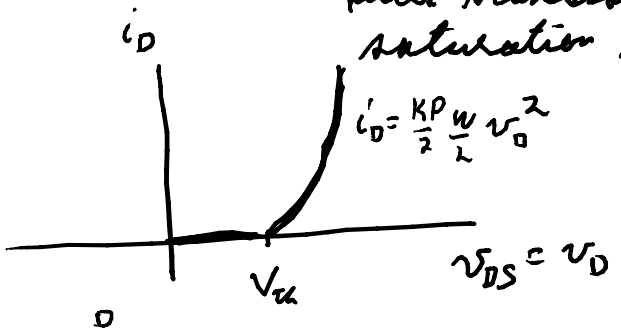




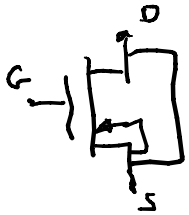
as a NMOS as a diode, $v_{DS} = v_{GS}$ then $v_{DS} > v_{GS} - V_{th}$

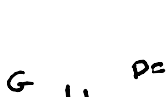


puts transistor in saturation if $v_{DS} > V_{th}$

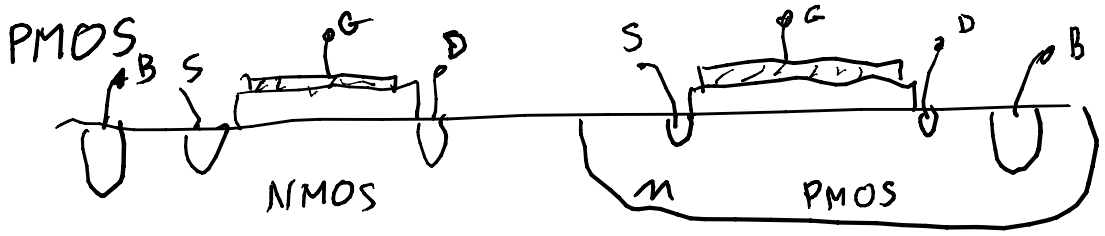


to make a capacitor



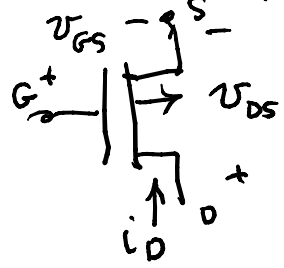


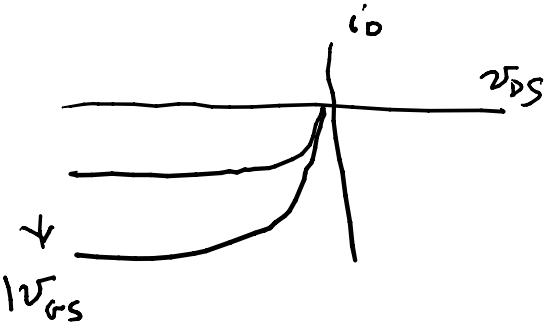
$C \approx C_{ox} W \times L$



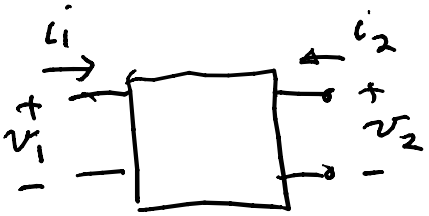
CMOS

PMOS





H parameters



$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = Y \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

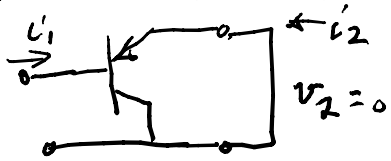
$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = H \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$$

$h_{21} \rightarrow h_{fe}$ for grd emitter BJT

$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0}$ = short circuit current gain of the 2-port

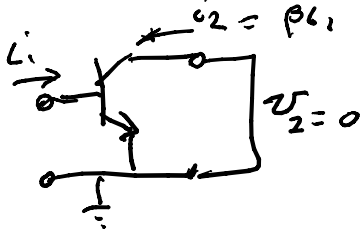
$h_{fe} = h_{21}$ forward grounded emitter

$h_{fe} \Rightarrow$ for



$i_2 = h_{21} i_1 + h_{22} v_2$

$i_2 = \beta i_1$



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for MOS we can operate sub-threshold then $|i_D| \approx 10^{-12}$ A pico amps range

p. 1129 $i_D = I_S e^{v_{GS}/nV_T}$ for $v_{DS} > v_{GS} - V_{th}$

$= \frac{W}{L} \cdot I_{D_0} e^{(v_{GS} - V_{th})/(nV_T)}$ $\left(\times \left[1 - e^{-v_{DS}/(nV_T)}\right]\right)$

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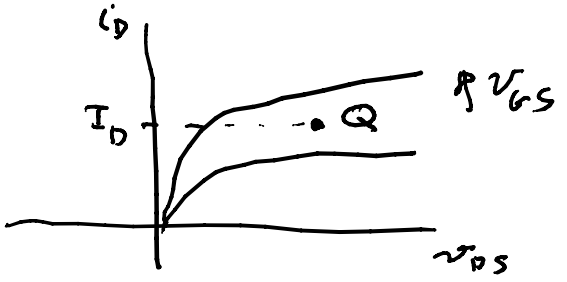
small signal NMOS (ignore Bulk but see p. 704) get π equivalent $\Rightarrow$ Y parameters



$$i_D(v_{GS}, v_{DS}) = I_D + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q (v_{GS} - V_{GS}) + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q (v_{DS} - V_{DS}) + \cdots$$

In saturation $i_D = \frac{KP}{2}\frac{W}{L}(v_{GS} - V_{th})^2(1 + \lambda v_{DS})$

$$\left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = 2 \cdot \left(\frac{KP}{2}\frac{W}{L}\right)(v_{GS} - V_{th})(1 + \lambda v_{DS})\Big|_Q = 2\frac{I_D}{(V_{GS} - V_{th})} = 2\frac{I_D}{V_{ov}}$$

$V_{ov} = V_{GS} - V_{th}$

$= y_{21} = g_m$

see p. 497

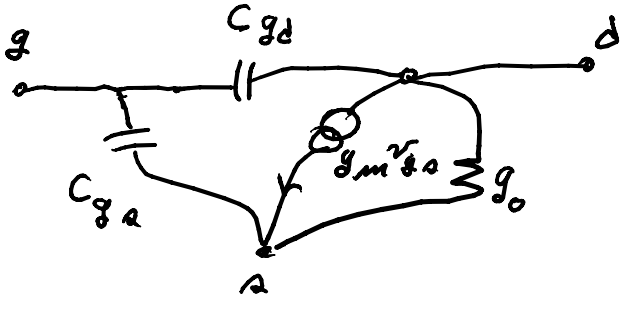
$$\left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \lambda\left(\frac{\frac{KP}{2}\frac{W}{L}(v_{GS} - V_{th})^2(1 + \lambda v_{DS})}{(1 + \lambda v_{DS})}\right)\Bigg|_Q = \frac{\lambda I_D}{(1 + \lambda V_{DS})} \approx \lambda I_D$$

$= g_o = y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1 = (v_{ga} = 0)}$

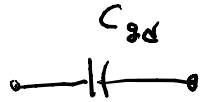
at very low frequencies $i_1 = 0 \Rightarrow Y = \begin{bmatrix} 0 & 0 \\ g_m & g_o \end{bmatrix}$

$i_D - I_D = i_d$, $v_{GS} - V_{GS} = v_{ga} = v_1$

$v_{DS} - V_{DS} = v_{da} = v_2$



$\Rightarrow$

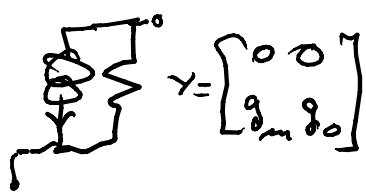


$$\Rightarrow Y_{C_{gd}} = sC_{gd}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$

+

$$= Y_{C_A} = \begin{bmatrix} sC_{ga} & 0 \\ 0 & 0 \end{bmatrix}$$

+ or

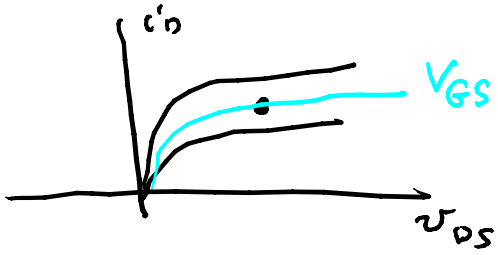


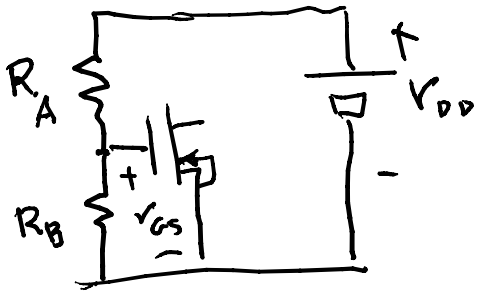
p. 706 for C_{ga} & C_{gd}

$$Y = \begin{bmatrix} sC_{ga} + sC_{gd} & -sC_{gd} \\ -sC_{gd} + g_m & sC_{gd} + g_o \end{bmatrix}$$

Bias of NMOS

as no DC current into gate can use a voltage divider to get V_{GS}





$$V_{GS} = \frac{R_B}{R_A + R_B} \cdot V_{DD}$$

$$= \frac{1}{1 + (R_A/R_B)} V_{DD}$$

free to choose one of R_A or R_B (choose large)