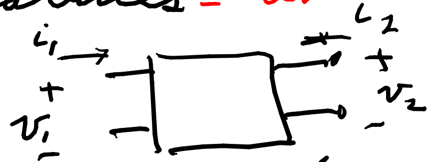
EE3034
09/20/11

MOS Transistors = Chapter 5

Y matrices = admittance matrix (small signal linearized)

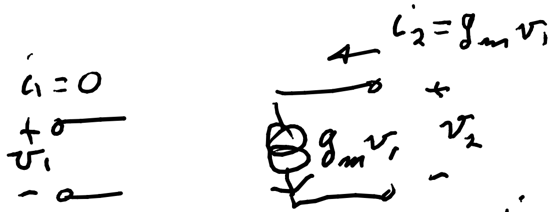


2-port linear

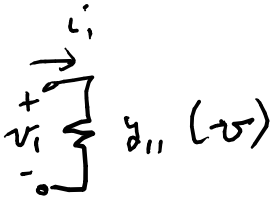
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = i = Y v = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

Equivalent circuits

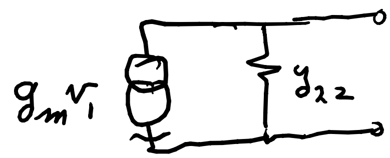
MOS Ex 1: $Y = \begin{bmatrix} 0 & 0 \\ g_m & 0 \end{bmatrix} \Rightarrow$

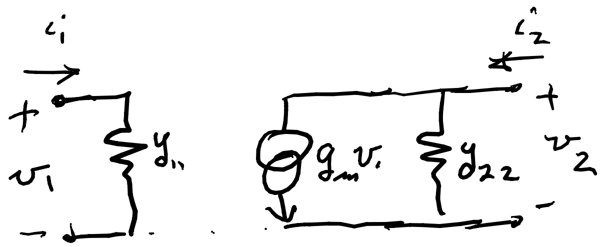


BJT Ex 2: $Y = \begin{bmatrix} y_{11} & 0 \\ g_m & y_{22} \end{bmatrix} \Rightarrow$ $i_1 = y_{11} v_1 + 0 \cdot v_2 \Rightarrow$

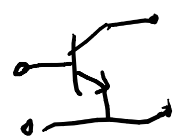


$i_2 = g_m v_1 + y_{22} v_2$





$Y = \begin{bmatrix} y_{11} & 0 \\ g_m & y_{22} \end{bmatrix}$

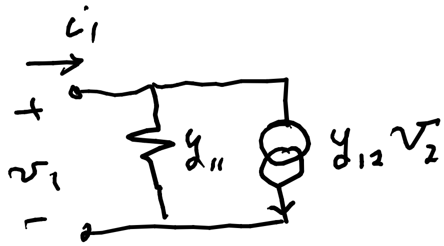


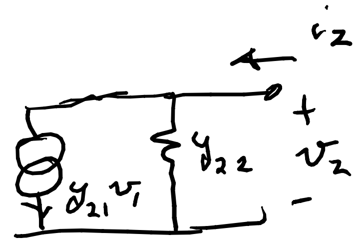
$Y = \begin{bmatrix} g_\pi & 0 \\ g_m & g_o \end{bmatrix}$

$g_m = \dfrac{I_C}{V_T}, \quad g_o = \dfrac{I_C}{V_A}$

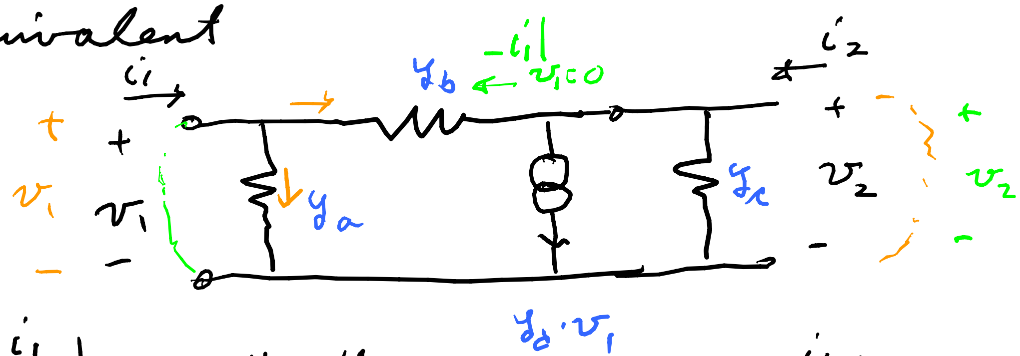
$g_\pi = \dfrac{g_m}{\beta}$

Ex 3: $Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$





π equivalent



$$y_{11} = \frac{i_1}{v_1}\Big|_{v_2=0} = y_a + y_b$$

(a short on port 2)

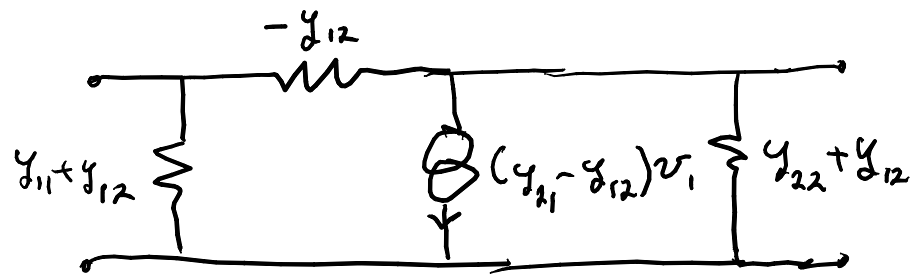
$$y_{12} = \frac{i_1}{v_2}\Big|_{v_1=0} = -y_b$$

(a short on port 1)

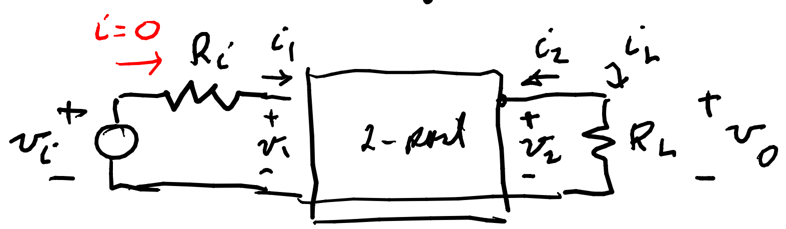
$\therefore$ given Y: $y_b = -y_{12}$, $y_a = y_{11} - y_b = y_{11} + y_{12}$

for y_c: $y_{22} = \frac{i_2}{v_2}\Big|_{v_1=0} = y_c + y_b \Rightarrow y_c = y_{22} - y_b = y_{22} + y_{12}$

y_d: $y_{21} = \frac{i_2}{v_1}\Big|_{v_2=0} = -y_b + y_d \Rightarrow y_d = y_{21} + y_b = y_{21} - y_{12}$



π equivalent circuit of a linear 2-port with Y matrix



find $\frac{v_o}{v_i}$

$$Y = \begin{bmatrix} 0 & 0 \\ g_m & 0 \end{bmatrix}$$

$$i_L \overset{KCL}{=} -i_2 \overset{\Omega}{=} G_L v_o \overset{KVL}{=} G_L v_2$$

$$i_2 = g_m v_1 \ (\text{from } Y) = g_m v_i \Rightarrow i_2 = g_m v_i$$

$$i_1 \overset{Y}{=} 0$$

$$-G_L v_o = g_m v_i \Rightarrow \frac{v_o}{v_i} = -R_L g_m = A_v$$

for $Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$

1) $v_i = R_i i_1 + v_1 = R_i(y_{11}v_1 + y_{12}v_2) + v_1$

2) $v_o = -R_L i_2 = -R_L(y_{21}v_1 + y_{22}v_o)$ as $v_2 = v_o$

1)⇒3) $v_i = R_i(y_{11}v_1 + y_{12}v_o) + v_1$

2)⇒4) $R_L y_{21} v_1 = (-R_L y_{22} - 1)v_o \Rightarrow v_1 = \frac{-(1+R_L y_{22})}{R_L y_{21}} \cdot v_o$

4)⇒3)

$$v_i = \left\{(R_i y_{11} + 1)\left[-\frac{(1+R_L y_{22})}{R_L y_{21}}\right] + R_i y_{12}\right\} v_o$$

$$= -\frac{R_i}{y_{21}}\left\{(y_{11}+G_i)(G_L+y_{22}) - y_{12}y_{21}\right\} v_o$$

$$= -\frac{R_i}{y_{21}}(y_{11}G_L + y_{22}G_i + G_iG_L + \Delta_y) v_o$$

let $\Delta_y = \det Y$
$= y_{11}y_{22} - y_{12}y_{21}$

$$\frac{v_o}{v_i} = -\frac{y_{21}}{R_i}\frac{1}{(y_{11}G_L + y_{22}G_i + G_iG_L + \Delta_y)}$$

(voltage gain of a loaded linear circuit)

ideal $y_{11} = y_{22} = y_{12} = 0$

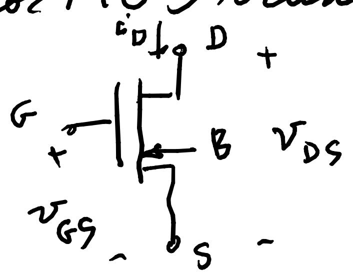
$\Delta_y = 0$

$$\frac{v_o}{v_i} = -\frac{y_{21}}{R_i} \cdot \frac{1}{G_L G_i} = -\frac{y_{21}}{G_L}$$

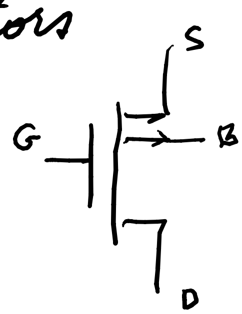
(as $R_i G_i = 1$)

checks as $y_{21} = g_m$ here

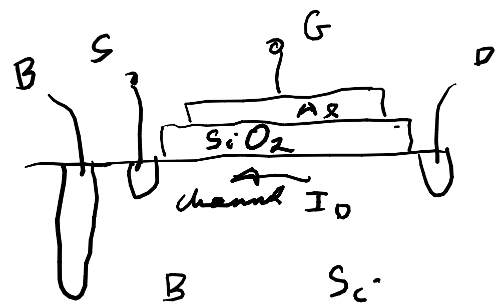
for MOS transistors

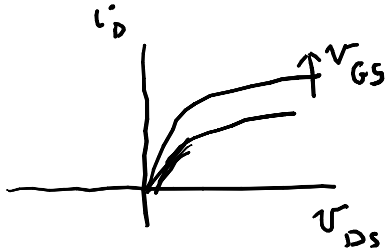


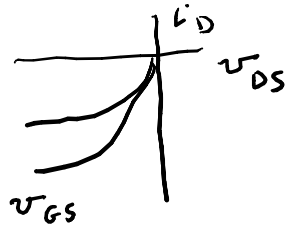
NMOS

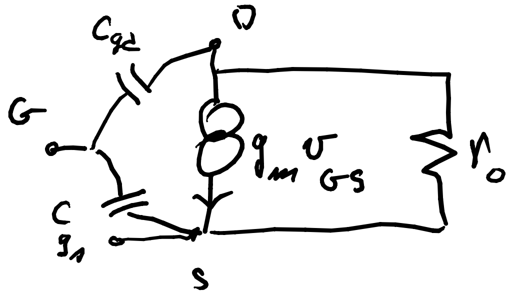


PMOS









$$Y = \begin{bmatrix} 0 & 0 \\ g_m & g_o \end{bmatrix}$$ at DC small signal

$$\Rightarrow \begin{bmatrix} C_d & -C_d \\ -C_d + g_m & C_d + g_o \end{bmatrix} = Y(a)$$