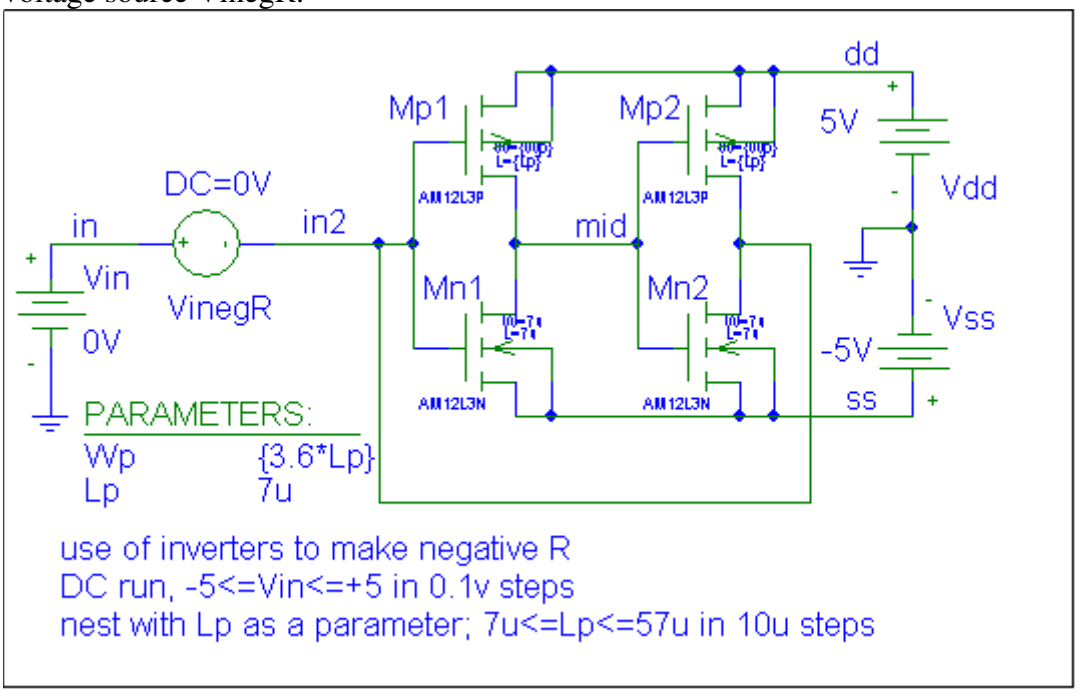
File: G:/coursesF08/610/610F09Hmwk1.doc RWN 09/06/09

610 Fall 2009 – Homework 1 Due ~~Tu~~ Th 09/~~15~~ 17/09

1. [50 points] [Spice runs]

a). Draw and run the following circuit in Spice and, in two separate plots to be turned in, plot in one the voltage at the node mid and in the other the current in the voltage source VinegR.



b). Turn off the nest and repeat the above circuit for the default value of Lp, 7u. For this circuit calculate from the Spice curves the voltage gain, ΔVmid/ΔVin at Vmid=0 (that is find the slope of the voltage transfer curve at the output origin) and the input current and admittance at VinegR=Vin=0. Comment on the linearity of this circuit.

2. [50 points] [circuit graph & Y matrices]

a) Consider the small signal equivalent for the above circuit by shorting the batteries (but keeping VinegR). Assume that all transistors have the same 2-port (=3-terminal) Y matrix (in MatLab notation with ; separating rows and ignoring bulks)

Ymos=[s(Cgs+Cgd) -sCgd; gm-sCgd go+sCgd]

Replace the transistors by this Ymos using three branches and three nodes for each. After combining equal parallel branches draw the circuit graph numbering the node in2 as I (with the ground as 0}, the voltage source in branch 1 and the capacitors in the next branches. Choose a tree which includes as many as possible of the branches to ground. Using that tree obtain the cut-set and tie-set matrices for (linear) small signal behavior.

b) Give the nodal admittance matrix and from it find the input admittance, yin(s), seen by the source VinegR. Evaluate at DC, that is for s=0. Compare with the results from the Spice runs.