EE303W
10/13/09

substrate bias

Eq. (4.33) p. 258 nMOS

$$V_t = V_{TO} + \gamma\left(\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right) \qquad 2\phi_f = 0.6V$$

PHISUB

$$\gamma = \frac{\sqrt{2|q|N_A\epsilon_{si}}}{C_{ox}}$$

assumes B-S diode is back-biased but can forward bias to close to 0.6 V

$N_A = NSUB$

$C_{ox}$ = capacitance/per unit area of the gate oxide

$C = \frac{\epsilon A}{t}$ ↗ needs $t_{ox}$

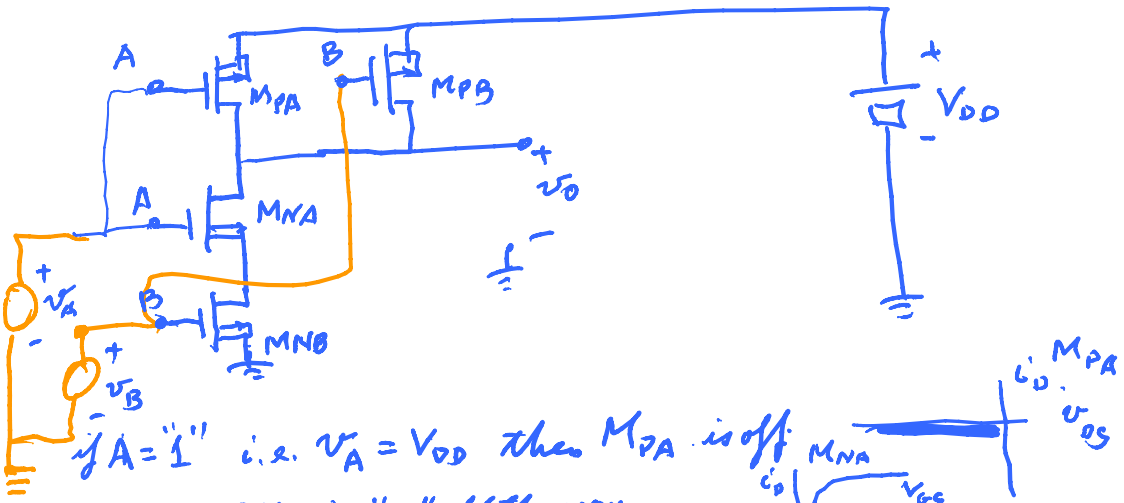
in saturation

$$i_D = \frac{KP}{2}\frac{W}{L}\left(v_{GS} - V_t\right)^2$$

↑ as $V_t(v_{SB})$ can control $i_D$ by $v_{SB}$


we can forward bias without drawing substrate current so can actually decrease $V_t$ over $V_{TO_n}$

p. 967 = CMOS gates fig. 10.13

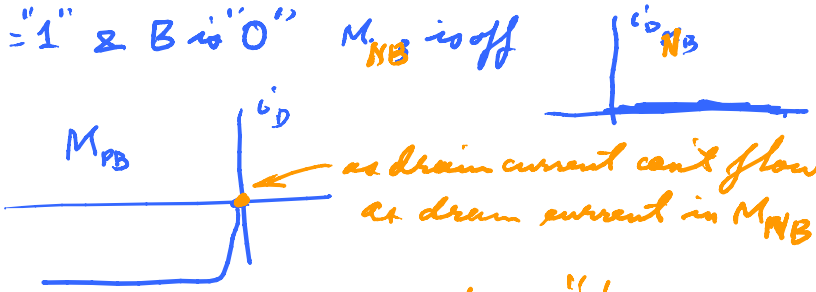



if A = "1" i.e. $v_A = V_{DD}$ then $M_{PA}$ is off & $M_{NA}$ is "on" all the way




and then if B is = "1" then $v_B = V_{DS}$ & $M_{PB}$ is off $\Rightarrow v_O$ = "0" = 0 V

if A = "1" & B is "0" $M_{NB}$ is off



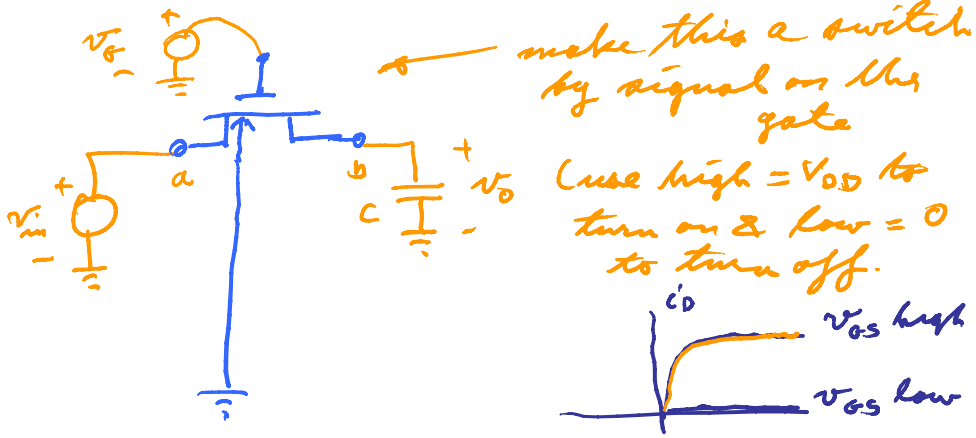

$\Rightarrow v_o = V_{DD} =$ "1"

if $v_A = v_B =$ "0" $v_o = V_{DD} =$ "1"

By the mathematics of the Sheffer stroke all binary logic functions can be realized by NAND gate.

The 4007 package was created for this (for CMOS gates)

alternate, use pass transistors

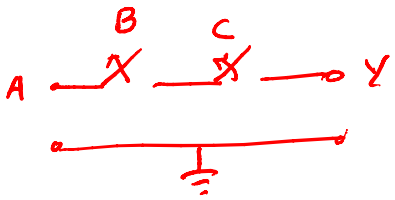



if $v_{in} > v_o$, a = D, b = S → current direction

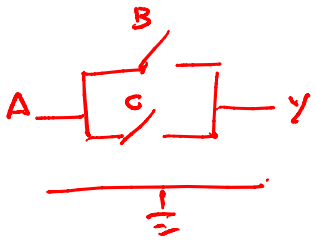
if $v_{in} < v_o$ a = S, b = D ← current direction

Here $v_G$ = gate voltage controls if we transfer $v_{in}$ to $v_o$ or not.

see p. 983 for pass transistor logic

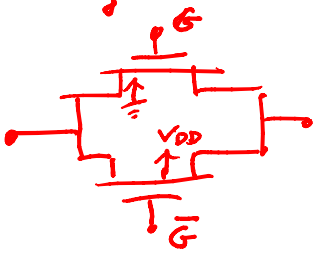



if B & C are closed
then $Y = A$




if B or C is closed
then $Y = A$

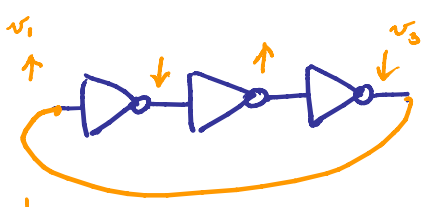
customarily one switch is 2 transistors





(= small resistance) of the switch we want large $W/L$

p. 996 has domino logic CMOS gates




$v_1 = v_3$ after some delay

frequency of changing gives the speed of a chip.

BIST = built in self test