

1. [60 points] [delay of inverters and NAND gate]
Use the 4007s to make CMOS inverters and NAND gates which are biased at $V_{DD}=10V$ and $V_{SS}=0$.
 - a) For a single inverter load it in a 10nFd capacitor. Calculate the delay time for switching from a low-to-high input, run a Spice simulation and compare the calculated with the simulated delay time.
For this use an input that is Vpulse with a rise time of 1femtoSecond and a long pulse width (set the initial voltage on the capacitor to VDD).
 - b) Using the same Spice circuit check the delay for a falling input (when the output is initially at VSS) and compare with that for the rising input.
Comment on any differences.
 - c) Cascade two of these inverters with the above load capacitor only on the second inverter. Compare the delay time seen at the input to the second inverter and the delay time for the full cascade, this for a rising input (when the output is initially at VSS).
 - d) Using the NAND gate of Figure 10.13, p. 967, load in the above capacitor and in Spice find the delay time when A is high and B transitions from high to low. Repeat when B is high and A transitions from high to low. Compare the two cases and discuss any differences.

2. [20 points] [bulk-source to i_D transconductance]
Equation (4.33) of p. 258 gives the effect of substrate bias on the behavior of MOS transistors. g_{mb} is in the equivalent circuit of Figure 4.41, p. 297.
 - a) From Spice models give the constants in Eq. (4.33) for the MNMOSIS and MPMOSIS ones as well as for the POLY2NMOS and POLY2PMOS (also in the bicmos12.lib file)[for the POLY2 transistors GAMMA needs to be calculated by Eq. (4.34) where N_A is the Spice NSUB].
 - b) For these transistors evaluate g_{mb} at a substrate bias of 0.1V magnitude (the sign being fixed by insuring the B-to-S diodes are back biased).

3. [20 points] [gain for bulk-source input]
Modify Figure 6.20 to have an input as the Bulk-to-Source voltage, V_{bs} , with the output as V_o [and V_{sig} & R_{sig} both removed, that is opened]. Draw the new equivalent circuit and find the voltage gain, $V_o/V_{bs}(s)$.