ENEE 303H Fall 2009 Final Exam

Open book, open notes. Your signature is required and certifies that the work is solely your own. 150 points total. If stuck be sure to go on to the next problem. Good Luck.

Use the following for transistor model Spice parameters:

For BJTs: $\beta = 100$, $V_T = 0.026V$ = thermal voltage, $|V_{BE}| = 0.7V$ when BE forward biased, $C\pi = 10pFd$, $V_A = 100V$ = Early voltage. .

For CMOS:transistors: VTOn = -VTOp=0 V, Cgs = 20 pFd, Cgd = 0

$KPn = KPp = 10^{-5} A/V^2$; $\lambda n = \lambda p = 0.02$

1. (60 pts, 30 min)

It is desired to bias the following Darlington pair via the three DC current sources shown. Assume that the identical BJTs are to be identically biased with Ic = 2mA.

   a) Give the values of the current sources to achieve this.
   b) Give g_π, g_m, and g_o for Q1 (these are the same for Q2)
   c) Draw the small signal equivalent circuit using the π-equivalent for Q1 and for Q2.
   d) Find y_{21} assuming port 1 is BE and port 2 CE.
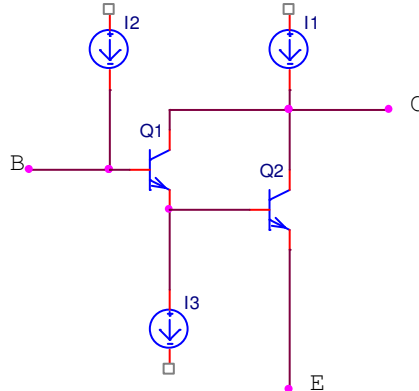
2. (60 pts, 30 min)

For the following circuit the voltages are measured with respect to a ground and the Out node has an open circuit load. Assume that V(Bulk) is at the lowest potential, Vss, of which V(in1) & V(in2) are always larger. Note from the above model data that VTO=0.

   a) Explain why if V(In1) is not equal to V(In2) then one transistor is off.
   b) When V(In1)>V(In2) give which nodes are d=drain and s=source for each transistor. Repeat for V(In2)>V(In1).
   c) Find V(out) as a function of V(In1) and V(In2).
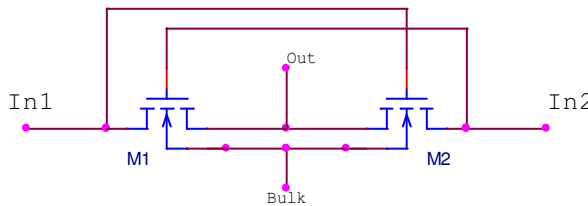
3. (15 pts, 10 min)
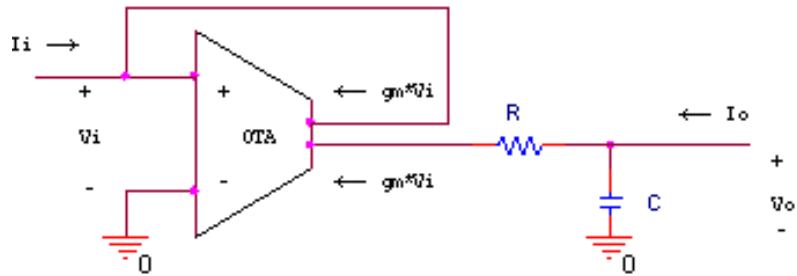


For this circuit assume the two output currents, I_{ota}, of the OTA are identical.
Recall that $\sinh(x)=(e^x-e^{-x})/2$.
a) If the OTA is described by $I_{ota}=\alpha I_T\sinh(V_i/(2V_T))$ give gm when biased at Vi=0 [where I_{ota} is directed as the OTA output currents shown; I_T is the tail current].
b) Find the 2-port admittance matrix Y(s) [valid for small signal vi] (in terms of gm, R, C). Here port 1 is the input one (on the left) and port 2 is the output one (on the right).

4. (15 points, 10 min)
For this circuit the op-amps are ideal and impedances non-zero.
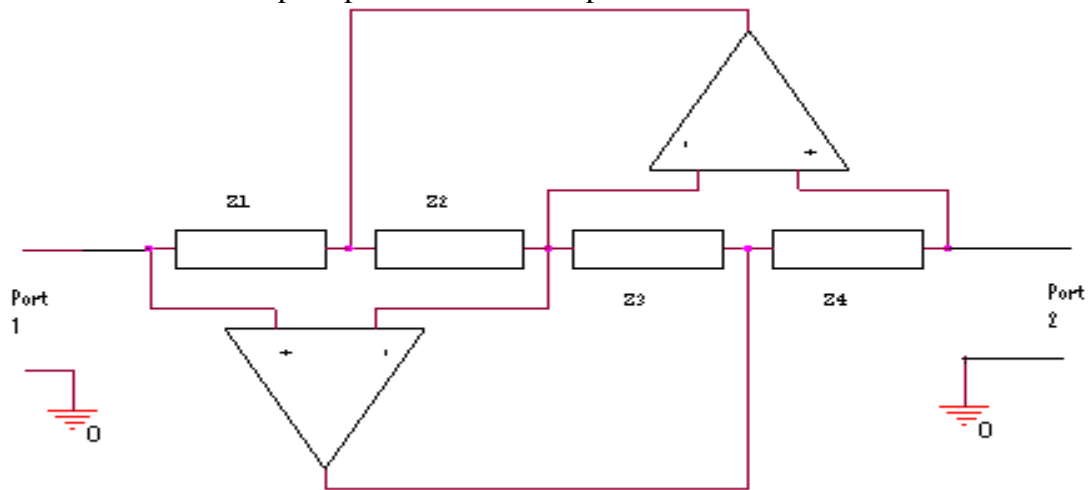
When port 2 is loaded in a short or an open yin(s)=0 or zin(s)=0 is seen at port 1.
a) When yload=0 determine which of yin or zin is 0.
b) When zload=0 determine which of yin or zin is 0.