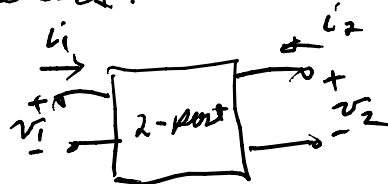


P. B-4 h Parameters:

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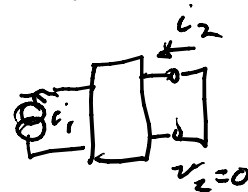
$h_{sr} = \text{small signal } \beta$



$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = Y \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = H \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

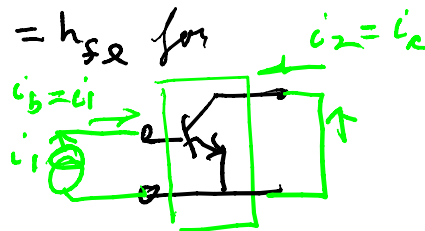
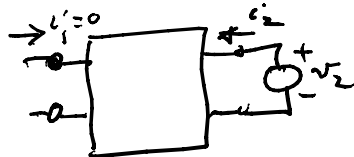
$$h_{21} = \left. \frac{i_2}{i_1} \right|_{v_2=0}$$



$$i_2 = h_{21} i_1 + h_{22} v_2$$

$= h_{sr}$ for

$$h_{22} = \left. \frac{i_2}{v_2} \right|_{i_1=0}$$



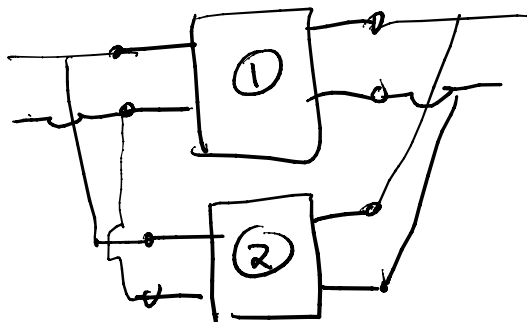
$= \text{open circuit output admittance}$

$$h_{11} = \left. v_1 / i_1 \right|_{v_2=0} \Rightarrow \text{short} = \text{short circuit input impedance}$$

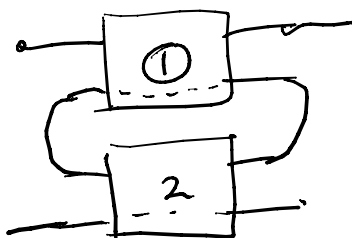
for G
P. B-5

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = G \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$$

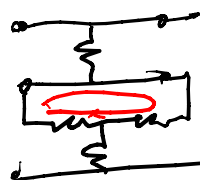
$$g_{21} = \left. \frac{v_2}{v_1} \right|_{i_2=0} = \text{open circuit voltage gain}$$



$\Leftarrow \text{adds } Y = Y_1 + Y_2$



$\Leftarrow \text{adds } Z = Z_1 + Z_2$
(need preserve eqs. before & after connect)



} no longer has the same Z

C_p & C_{π}

C_{je0} = emitter junction C

p. 490

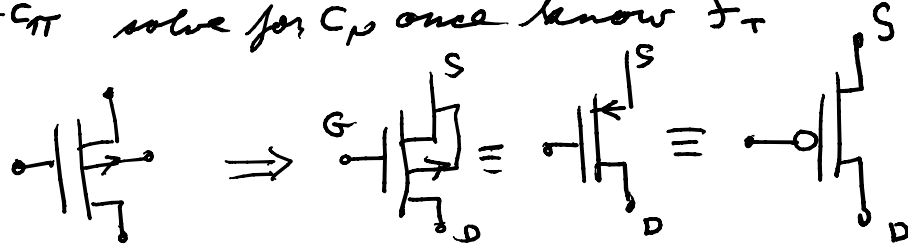
$$C_{\pi} = C_{d2} + C_{je}$$

$$C_{je} = 2 C_{je0}$$

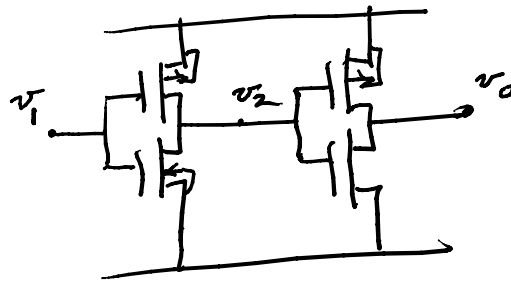
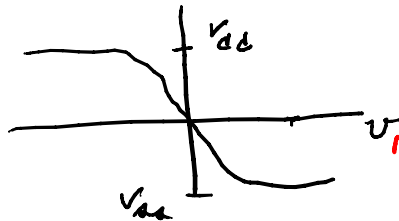
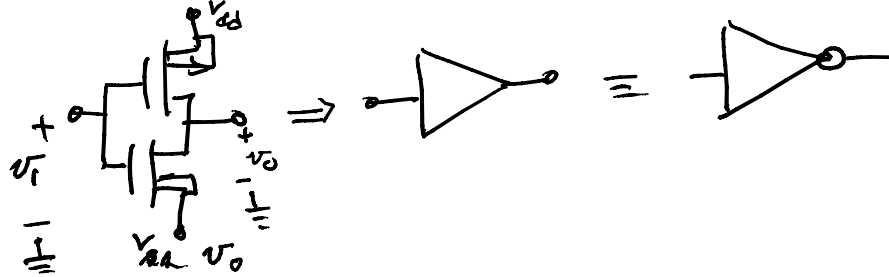
$$C_{d2} = \tau_f g_m$$

$$\omega_T = \frac{g_m}{C_p + C_{\pi}} \text{ solve for } C_p \text{ once know } f_T$$

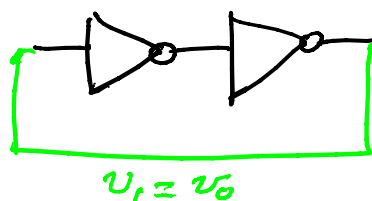
Notation



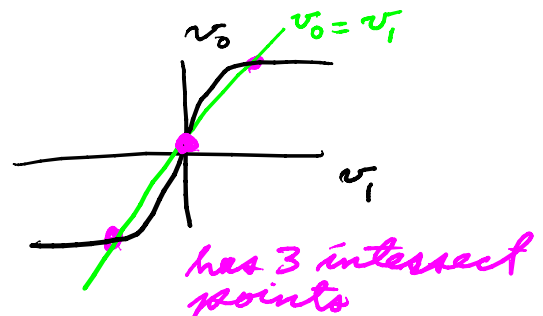
For the inverters

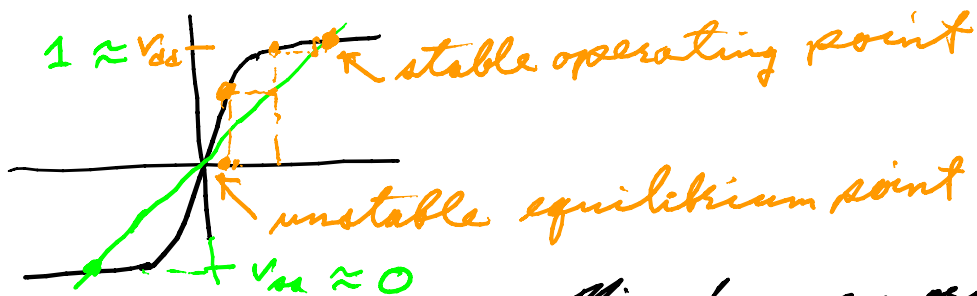


Connect output to input



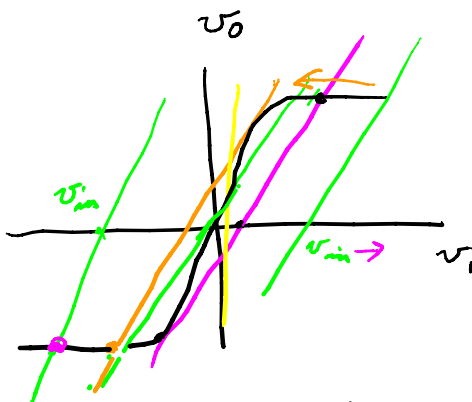
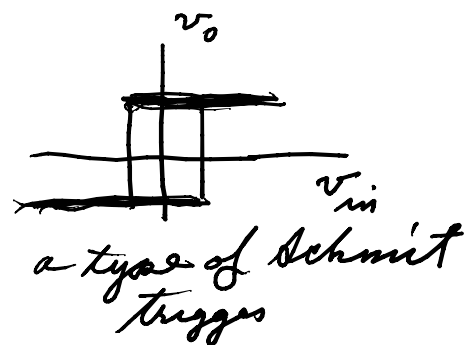
transfer curve of a cascade of inverters





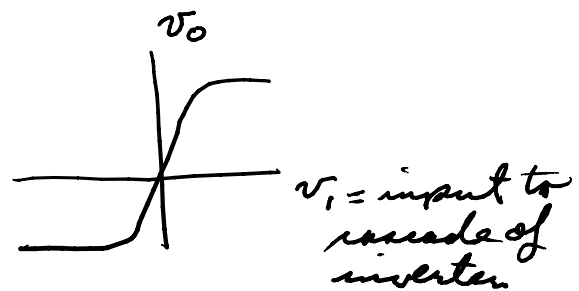
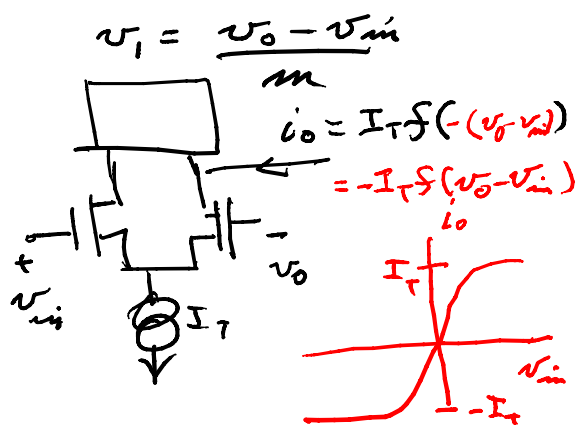
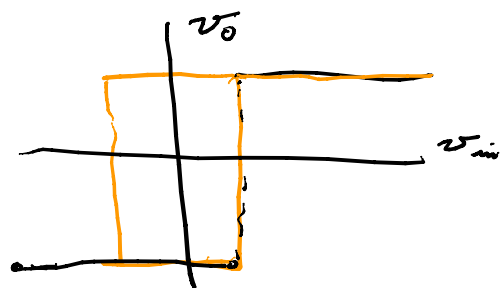
More for memory if can get signals in

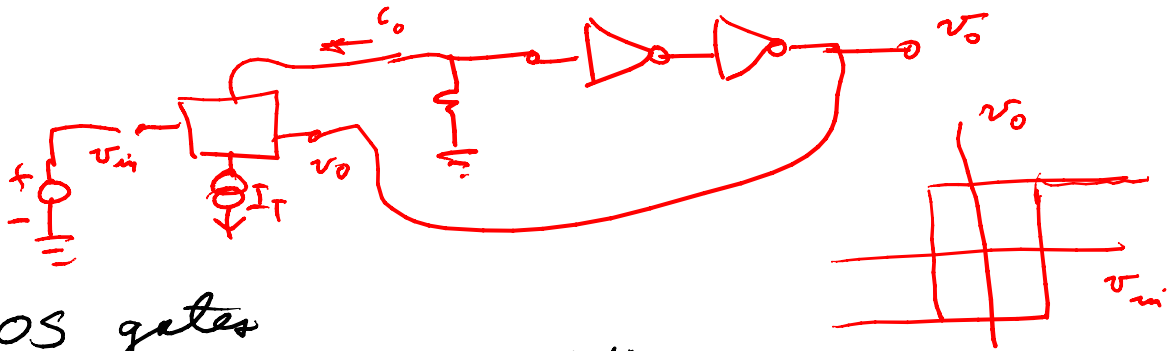
To create hysteresis with this



Load line equation

$$v_o \approx m v_i + v_{in} \quad m > 0$$





CMOS gates
p. 967 Fig. 10.13 = NAND

