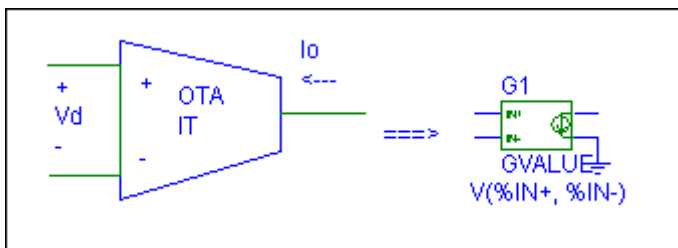


303 Fall 2008 – Homework 6 Due Tu 10/14/08

1. Using 4007 packaged transistors (=CA3600 Spice package) create the CMOS NOR gate of Figure 10.12, p. 967. Connect a capacitor load from the output, node Y, to ground and bias with VDD=5V. For the capacitor use a MOSFET P & N parallel connected capacitor (the capacitor is formed by connecting the drain to the source with that connection for one lead and the gate lead for the other). Do a Spice transient analysis run with the inputs from piecewise linear voltage sources set to give the logic signals in the combinations needed to check that the circuit is a NOR gate; be sure to use large enough pulse widths so that the output settles as well as small, pSec, rise and fall times. Give the delay through the gate using the delay time as the time between 50% amplitude points of the input and output. .
2. Repeat problem 1 above for the NAND gate of Figure 10.13.
- 3.

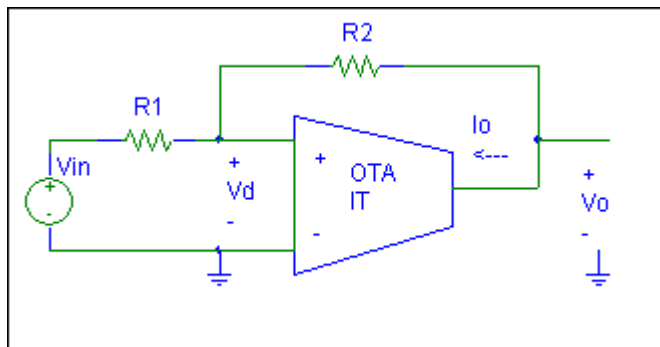


An OTA = (Operational Transconductance Amplifier) is a differential pair with an “active” load to give the output to be the difference current of the pair collector currents. In the NPN BJT pair case the load is shown in Figure 7.32 and the current difference,  $I_o$ , is derived from Equations (7.72) to be

$$I_o = -I_T \cdot \tanh(V_d / (2V_T))$$

Where  $I_T$  is the tail current (called simply  $I$  in the text)

In Spice the idealized BJT OTA can be simulated using a GVALUE component (in the ABM library) with the expression for  $I_o$  as the gain. With these facts in mind consider the following circuit for which the output voltage,  $V_o$ , is measured with no load (no current in the right lead)



(continued on next page)

- a) For this circuit show that the load line equation, is (where  $G1=1/R1$ )  
$$I_o = -G1(V_d - V_{in})$$
- b) Sketch the OTA curve of  $I_o$  versus  $V_d$  and the load line curves of  $I_o$  versus  $V_d$  for several important values of  $V_{in}$ . From that show that this circuit has hysteresis. Calculate the smallest  $R1$ , call it  $R_{min}$ , such that hysteresis will result (for this you can set the tangents equal for the OTA curve and the load line). Find the voltages  $\pm V_j$  at which the hysteresis jumps, Sketch  $I_o$  versus  $V_{in}$  showing the hysteresis.
- c) Choose  $R1 = 2R_{min}$ ,  $R2 = R1$ ,  $I_T = 104\mu A (=4 \times 26\mu A)$ ,  $V_T = 26mV$ , and run a transient response in Spice using an input voltage that is triangular via the piecewise linear voltage source, VPWL, starting at 0, going slowly negative to twice the hysteresis negative jump point and then to positive twice the hysteresis positive jump point, and then back to the most negative value. Plot  $I_o$  versus  $V_{in}$ .
- d) Calculate  $V_o$  versus  $V_{in}$  and sketch the result; compare with Spice results.