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*.model CA3600E
*14-pin DIP: pin#1 #2 #3 #4 #5 #6 #7 #8 #9 #10 #11 #12 #13 #14
*
| | | | | | | | | | | | | |
.subckt CA3600E-X p01 p02 p03 p04 p05 p06 p07 p08 p09 p10 p11 p12 p13 p14
*
      RCA      pid=CA3600
*
      89-07-21 pwt

* The RCA data sheet was used for this model.

* BE SURE to keep pin #14 at the most positive potential w.r.t any other pin!
* BE SURE to keep pin # 7 at the most negative potential w.r.t any other pin!

m_N1 p08  6 p07 p07 nch      ; device N1
m_N2 p05  3 p04 p07 nch      ; device N2
m_N3 p12 10 p09 p07 nch      ; device N3

m_P1 p13  6 p14 p14 pch      ; device P1
m_P2 p01  3 p02 p14 pch      ; device P2
m_P3 p12 10 p11 p14 pch      ; device P3

* Input protection circuits from Fig. 34

rx03 p03  3 r_zap 1          ; input protection on pin #3
dx3p p03 p14 d_zap
di3p  3 p14 d_zap
di3n p07  3 d_zap

rx06 p06  6 r_zap 1          ; input protection on pin #6
dx6p p06 p14 d_zap
di6p  6 p14 d_zap
di6n p07  6 d_zap

rx10 p10 10 r_zap 1          ; input protection on pin #10
dx1p p10 p14 d_zap
di1p 10 p14 d_zap
di1n p07 10 d_zap

d1 p07 p14 d_body           ; supply protection diode (D5 in Fig. 34)

* MOS characteristics derived as follows:
*
*      Id vs Vgs from Fig. 3 and 6 (using Parts as an aid)
*
*      output capacitance hand adjusted using simulations
*
*      Miller capacitance and output impedance hand adjusted using
*      simulations to match Fig. 10 and 11

.model nch nmos (Level=1 Tox=300n Uo=600 Kp=20.54u W=144u L=8u Vto= 1.3
+
      Lambda=15m Cbd=4p Cbs=4p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)
.model pch pmos (Level=1 Tox=300n Uo=300 Kp=10.32u W=328u L=8u Vto=-1.5
+
      Lambda=15m Cbd=8p Cbs=8p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)
.model r_zap res (r=1.73K)
.model d_zap D (Is= 1p Rs=1 N=1 Xti=3 Eg=1.11 Cjo=.01p M=0 Bv=20 Ibv=.1u)
.model d_body D (Is=15n Rs=1 N=1 Xti=3 Eg=1.11 Cjo=10p M=.5 Vj=.75
+
      Fc=.5 Isr=.15n Nr=2 Bv=20 Ibv=100u)
.ends
*$

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