ENEE 417 - Fall 2002
Weeks #6-#8
Design #3: Inverter Circuit Designs: layout and use

In this experiment the CMOS inverter will be used for various functions and activities.
1 Design a three stage and a five stage ring oscillator. Run Spice simulations and then construct and test the circuit using the 4007 transistors.

2. Insert equal capacitors between the stages and note the effects. Then insert one Super capacitor. Vary the bias voltage and see how the circuit operates in subtheshold.

3. Do a MAGIC layout for 1.6u transistors of a three stage and a five stage ring oscillator and do a Spice extraction to check your layout results versus a PSpice run used for design (for the 1.6u MOSIS transistors).

4. Simulate using PSpice Nauta's CMOS transconductance element (which uses only inverters) using 1.6u MOSIS technology. Do a VLSI layout and a Spice extraction to check your layout. Do a circuit analysis of the circuit to make sure you understand its operation. Check to see if the circuit will work as desired in subthreshold operation.

5. Insert your inverter and Nauta's circuits into 1.6u pads. Prepare for a MOSIS submission (those who wish to have theirs fabricated may actually submit).

6. Write a one to two page report summarizing your study.

Reference:
CMOS inverters - any standard electronics textbook
Nauta's circuit:

B. Nauta and E. Seevinck, "Linear CMOS Transconductance Element for VHF Filters," Electronics Letters, Vol 25, No. 7, March 30, 1989, pp. 448 - 450.