ENEE 417 - Fall 2002

Weeks #4 - #5

Design #2: CMOS Threshold Voltage Extractor

In this experiment a MOS circuit will be designed, constructed, and tested, that has as its output the threshold voltage of an MOS transistor.

1. Read the article: M. G. Johnson, "An Input-Free VT Extractor Circuit Using a Two-Transistor Differential Amplifier," IEEE Journal of Solid-State Circuits, Vol. 28, No. 6, June 1993, pp. 704-705.
2. Based on that paper design a threshold voltage extractor using the 4007 MOS transistors available in the Laboratory. Do Spice runs to check your design and construct and test your extractor. Consider the effects of different substrate voltages and means to handle both P and N MOS. For Spice computer runs note that the models to use are those of the equivalent RCA 3600 transistors in the PSpice model library CA3600.lib.
3. Using LabView save in the computer various graphs, including the MOS ID vs. VDS with VGS as a parameter and your VTO extractions.
4. Write a one to two page report summarizing your study.
5. Be sure to get your TA right away a parts list for your base paper so that items not on hand can be considered in time.
6. Choose an oscillator, current mirror, or differential pair from a textbook or journal paper for your third design.