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ENEE 302 Possible to do items #6

1. Design a 2-input CMOS NAND gate, biased by  $V_{dd}$  and ground, such that if initially both A and B inputs are at 0 and the B input changes to a 1, the output voltage will be  $V_{dd}/2$  when the B input hits  $V_{dd}/2$ . Check this with Spice. Determine the output voltage for your design when initially  $A=1$ ,  $B=0$ , and B changes to a 1 as it passes through  $V_{dd}/2$ . Also do a set of runs for various PMOS width parameters to see the effect of changing the PMOS widths.
2. Do a similar design as 1. above for a 2-input CMOS NOR gate.
3. Using your CMOS circuit of 2, design a CMOS NOR SR (flip-flop) latch and check its operation in Spice. Repeat by designing a CMOS NAND SR latch.