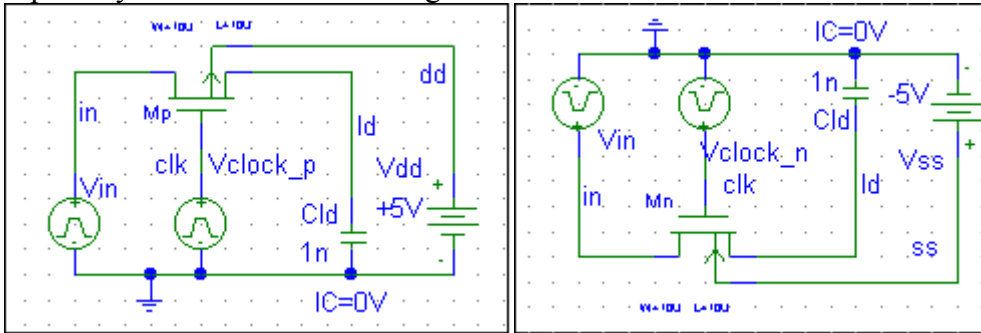File: 302f0_04 RWN   09/18/00
ENEE 302 Possible to do items #4.

1.   For the two following transmission gates do Spice runs for various input_pulse-clock_pulse-capacitor_IC combinations. Note the possible clock feedthrough effects. For one set of these conditions vary the transistor width parameters and see the effects especially on the clock feedthrough.

2.   Tale the two transmission gates of 1. above and use them together with complementary clocks as per the following. Run similar curves to those run in 1. above. Investigate differences and give the advantages and disadvantages of this configuration.
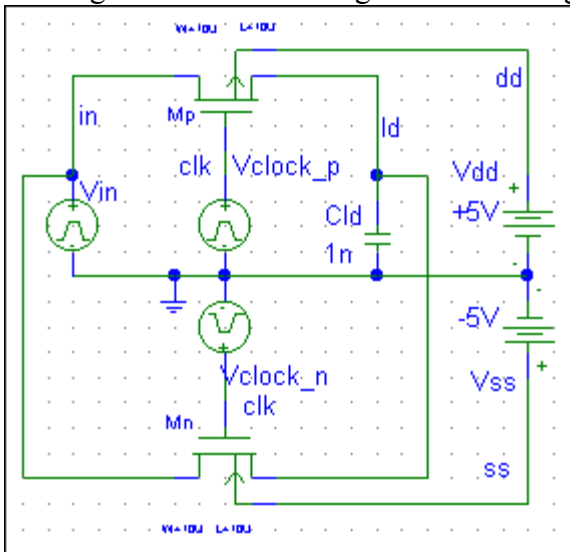
3.   In 1. above disconnect the substrates (=bulk) from their bias sources and connect them for a set of runs to the capacitors, and then for another set of runs to the input voltage sources. Check the differences from 1. above and especially monitor the bulk currents, IB, of the transistors.