High Temperature Modeling and Characterization of 6H SiC MOSFETs

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(abstract)
SiC offers the potential to provide high power, high temperature electronics. Our two-dimensional is used to model the current voltage characteristics of a 6H-SiC MOSFET as a function of temperature, from 25°C to 200°C.

(intro)
In our previous paper[1], we developed a new detailed mobility model for Silicon Carbide (SiC) MOSFETs. The new model explicitly accounts for the contribution of ionized impurities, surface phonons, interface states and surface roughness scattering, as well as high fields as a function of position and temperature. We then used numerical methods to design a new two-dimensional device simulator specifically for SiC MOSFETs. The new device simulator was based on the drift-diffusion model of carrier transport. Using the new simulator, we demonstrated agreement of the model predictions and measurements for 6H SiC MOSFETs at room temperature only. In this communication, we expand upon our previous work by applying our device model to MOSFETs operating at high temperatures. We compare the model predictions with the actual device measurements from room temperature to 200°C. From the combined use of the model and experiment, we present a quantified description of the role of temperature-dependent interface trap occupation and its effect on SiC MOSFET operation.

(method)
We experimentally characterized 4µm 6H SiC MOSFETs[1] at room temperature, 100 and 200°C. One interesting feature was that as the temperature increases, the measured drain current increased, and the threshold voltage decreased. Other researchers reported similar results[2]. Of course, this is contrary to what is normally observed in standard silicon devices. In this work we explain this behavior by relating temperature dependent device performance to mobility and interface state charging.

Using Matheson’s rule the inverse of the total low-field mobility can be written as the sum of the inverses of the individual mobility mechanisms.

\[
\frac{1}{\mu_{LF}} = \frac{1}{\mu_B} + \frac{1}{\mu_{Cit}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}
\]

In our previous work we presented a detailed device model for each of the terms in equation (1)[1, 2]. In the present work we pay particular attention to the temperature dependencies of our mobility model. Since the analytical expressions have already been given[1], here we qualitatively explain the physics which gives rise to the temperature dependence of each term.

The first term on the right hand side (RHS) of equation (1) represents the low-field bulk mobility \(\mu_B\). This mobility is largely affected by ionized impurities and acoustic phonons. As the temperature increases, the acoustic phonon scattering rate increases and hence \(\mu_B\) decreases.

The second term on the RHS of equation (1) represents mobility dependence on surface scattering from trapped interface charge. Interface charge trapping is quantified with Fermi statistics, which show that as the temperature increases, the quantity of trapped interface charge \(N_{it}\) decreases. As a result, coulombic scattering from trapped interface charge decreases with increasing temperature, which gives rise to an increase in the interface-trapped charge mobility term. We show in Figure 4 below that this term plays a vital role in 6H SiC MOSFET behavior.

The third term on the RHS of equation (1) represents the mobility contribution from surface acoustic phonons \(\mu_{ph}\). This contribution decreases with temperature since the surface phonon scattering rate increases with temperature as described by Boson statistics, which predicts that increased temperatures give rise to higher phonon populations and thus higher scattering rates and lower mobility.

The fourth term on the RHS side of equation (1) corresponds to surface roughness scattering. In contrast with phonon scattering and coulombic scattering,
the surface roughness scattering rate does not have a strong explicit temperature dependence, we therefore take our surface roughness mobility term \( \mu_{sr} \) to be temperature independent.

Device simulations were performed employing the aforementioned mobility model. The device simulator, which was written specifically for 6H-SiC MOSFETs, was based on the drift-diffusion equations. The simulator numerically solved the Poisson, electron-current continuity and hole-current continuity equations self-consistently. The simulator also accounted for the effects of temperature resulting from internal power generation, as well as temperature variations from the outside world. In addition to the effects of temperature on mobility, the simulator accounted for its effects on intrinsic electron concentration, bandgap, donor ionization work function differences, and interface state occupation. Accounting for these attributes yielded unique challenges for SiC simulation. These challenges were overcome by developing new numerical iteration methods, scaling of variables, and the use of new physical models.

Values for the bulk mobility and surface phonon terms are dictated by the structure of the lattice, and therefore we took the parameters in these models as fixed. These fixed values, which include the effective masses, density, velocity of sound and dielectric constants, were taken from the literature[4, 5]. On the other hand, the parameters in the interface charge model and the surface roughness model are dictated by the process. We therefore extracted the relevant parameters in these models by requiring simulated values of terminal currents to match experimental values.

To understand and quantify behavior at elevated temperatures, we first had to make sure our room temperature model was accurate. Thus, we first simulated the room temperature I-V data and extracted the process-dependent parameters. The first parameter extracted was the fixed oxide charge density \( N_f \). This is achieved using the \( I_D - V_{GS} \) data. When the MOSFET is in the subthreshold (\( V_{GS} << V_{th} \)), electrons are not plentiful at the surface, so few traps near the conduction band edge are occupied. As a result, the interface trap charge is dominated by the presence of electrons in the midband region. In addition, screening is not a factor because of the low volume of electrons at the surface. Given the above conditions, \( N_f \) uniquely affects I-V characteristics, and its value was extracted by adjusting \( N_f \) until agreement was achieved between simulation and experiment in the subthreshold region.

Moving up the \( I_D - V_{GS} \) curve, electrons begin to populate the interface trap states near the conduction band edge as the gate-source voltage is increased, and the modeling terms \( D_c \) and \( \xi_e \) begin to play a role. We use the experimental findings in [? , ?] to obtain an initial range of \( \xi_e \) to be between 0.1 and 0.2 eV. The value for the band edge interface trap density of states peak, \( D_c \), is obtained by requiring that the transition region from subthreshold to threshold agrees with experimental observation.

Once the \( I_D - V_{GS} \) curve moves from subthreshold to well above threshold, the channel concentration increases dramatically and electron screening of interface states becomes important. Our model accounts for this phenomenon with the electron screening parameters, \( n_{CUT} \) and \( \zeta_{CUT} \). Values for these parameters are therefore obtained by requiring agreement between experiment and simulation at the onset of strong inversion.

The extracted values for \( D_c \), \( \xi_e \), \( N_f, n_{CUT} \) and \( \zeta_{CUT} \) are given in Table 1. The resulting I-V curves comparing experiment and theory using our model are shown in Figure .

With the process dependent model parameters extracted, we were then ready to test the temperature dependence of our simulator, while taking the process-dependent parameter values as fixed. We simulated device operation at 100°C and 200°C without changing anything in our model. The variations in temperature were included only by setting the explicit temperature variable in our model to 100°C or 200°C, respectively[1].

The resulting \( I - V \) curves are given in Figures 2 through 3. The model results are in good agreement with experiment for almost the entire range of temperatures and \( V_{GS} \). This agreement was achieved with absolutely no high temperature optimization.

This accomplishment helps to validate the robustness and completeness of the models used to characterize the transport physics of the SiC MOSFETs. This agreement argues strongly that our model is accurate. The midband density of states and fixed oxide is likely correct since the \( I - V \) curves match in subthreshold. Additionally, the band edge interface trap values and mobility models are likely to be accurate since the knee and above-threshold portions of the \( I_D - V_{GS} \) data match. Most importantly, the agreement shows that the temperature dependence of the model is correct. Not only is the trend of increasing current with higher

| \( D_c \) (cm\(^{-2}\) eV\(^{-1}\)) | 1.52 x 10\(^{12}\) |
| \( \xi_e \) (eV) | 0.11 |
| \( N_f \) (cm\(^{-2}\)) | (+) 3.80 x 10\(^{11}\) |
| \( n_{CUT} \) (cm\(^{-3}\)) | 3.65 x 10\(^{11}\) |
| \( \zeta_{CUT} \) | 1 |

Table 1: Process-dependent modeling parameters for 6H-SiC MOSFETs.
temperature observed in our simulations, but precise agreement is temperature is obtained. Only minor divergence from the experimental data at high $V_{GS}$ values suggest that either the effective screening may be too low.

Figure 4 helps to explain the observed increase in current with temperature. The figure shows the calculated trapped interface charge as a function of position at 27, 100 and 200°C. From the figure we see how the trap density decreases with increasing temperature. This decrease helps to explain both the reduction in threshold voltage, and the increased mobility and current as the temperature rises.

In summary, we have developed a device simulator and physical model for explaining and predicting the temperature behavior of 6H-SiC MOSFETs. The model agrees well with experiment and should be of use in designing 6H-SiC MOSFETs, and should prove to be an excellent starting point for the development of modeling tools for 4H-SiC devices as well.

References


Figure 3: Linear scale of drain current versus gate-source voltage at room temperature, 100 Celsius, and 200 Celsius for a drain-source voltage equal to 0.25 Volts.

Figure 4: Occupied interface trap density of device C1 at $V_{GS} = 6V$, $V_{DS} = 0.5V$ for various temperatures.