For PSPICE simulation, you need:

1. Install the course library: EE408D4T.slb. It's a self extraction file, available on our
   Course web site.
2. The procedure of install the library is described in detail on the home page on our
   course web site.
3. After the library is built to your PSPICE, you need to build circuits hierarchically.

Procedures to build a hierachial circuit:(Example)

1. Build your NAND gate by transistors.
2. Test your NAND gate works well.
3. Remove the Signal or Power supply of your NAND gate. Instead, go to the library:
   port.slb, get the part: IF_IN, IF_OUT, or INTERFACE. Give the names for those ports.
   Also, for some connections, like your Vdd, you can use bubble as the proper part in PSPICE.
4. Goto **File-->Symbolize**, give the name of your gate, like AnandB. Put this new parts
   into a library, let's say :myGate. save the myGate to Userlib folder, or whatever folder you
   want.
5. Open a new Schematic file to use the block AnandB you just built to build a new circuit.
   In order to do this, you need to repeat the procedures of adding a library file to your
   PSPICE, as shown in the first part of this instruction.

For LASI, you need(The simplest way to do the layout):

1. Build the cell of NAND, NOT, NOR(refer book Chapter 11). You can use the Cell in the
   LASI library, too. But you must make sure that you understand what part is your PMOS, what
   par is your NMOS, and where is the body for each of them, how do they connected.
2. After you get your unit(either built by yourself or by choosing the one in the LASI
   library), you need to make metal connections between the input and output of your gate,
   in order to realize the proper logic functions of your circuit.
3. The communication of the signal is realized by the metal layer. Make sure there are proper
   contacts between the active region and the metal layer, or between the poly gate and the metal
   layer. Also, if the view of your layout has cross line of the metal wires, remember to use
   metal2 layer to avoid incorrect communications.
4. The input signal of the total circuit is get from the PAD. Recall the homework3 layout
   problems. We need to put our circuit in a PAD frame, and the input and output are connected
   to different PAD through metal layers. One PAD will become one leg after your chip is packaged.

BTW, We won't use all of the PAD of course. Don't worry about those redundant PADs.

After all, for the layout part, you need to show:

1. the whole chip, with PAD connection
2. Each types of gates' layout
3. The layout of your gates without shown the PAD connection (The reason is: It is impossible
   to show the detailed connection large enough to tell it's correct or not if it is shown
   with PADs)