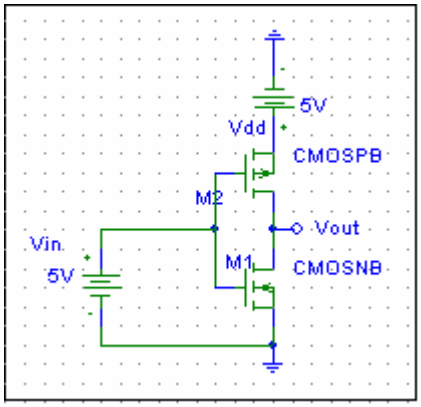
ENEE408D HW7 Solution Spring 2003

Problem 11.1

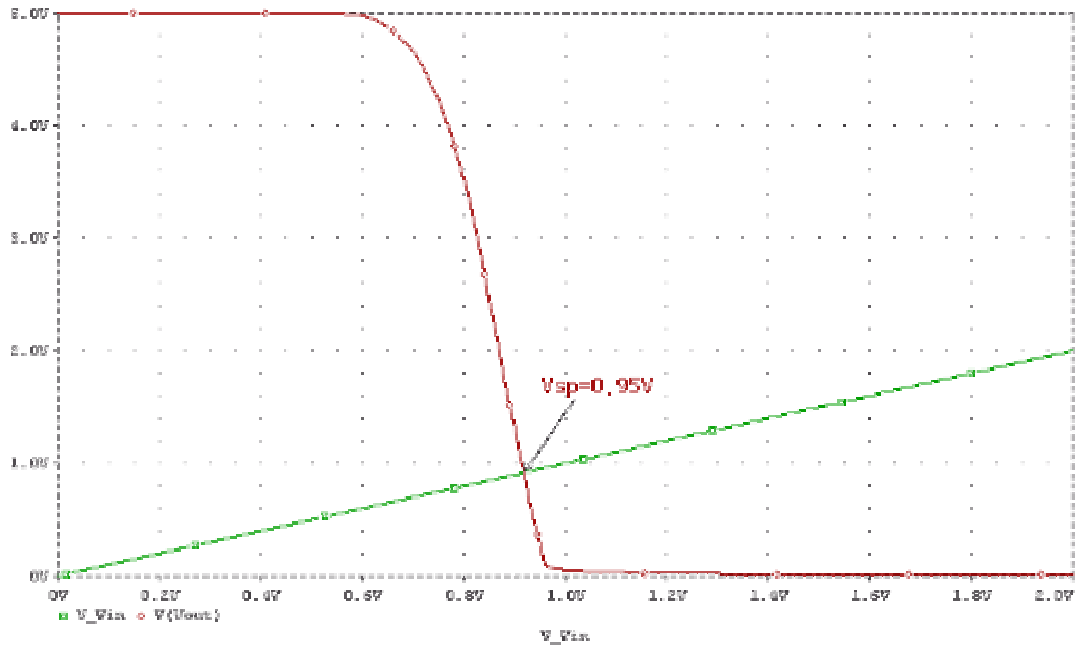
From equation (11.4), with V_{SP} approximately equal to VTHN, βn should be far larger than βp. In a basic inverter, for both NMOS and PMOS, the length of devices is same and Wn = 400μm, Wp=3μm. Assume KPn = 3KPp, VDD = 5V, V_{THN}=V_{THP}=0.9V ,

$V_{SP} = (20\ V_{THN} + VDD - V_{THP})/ (1+20) \approx 1.05V$



PMOS: 3/2, NMOS: 400/2

While doing simulation, need to use the DC sweep to observe the Vsp.

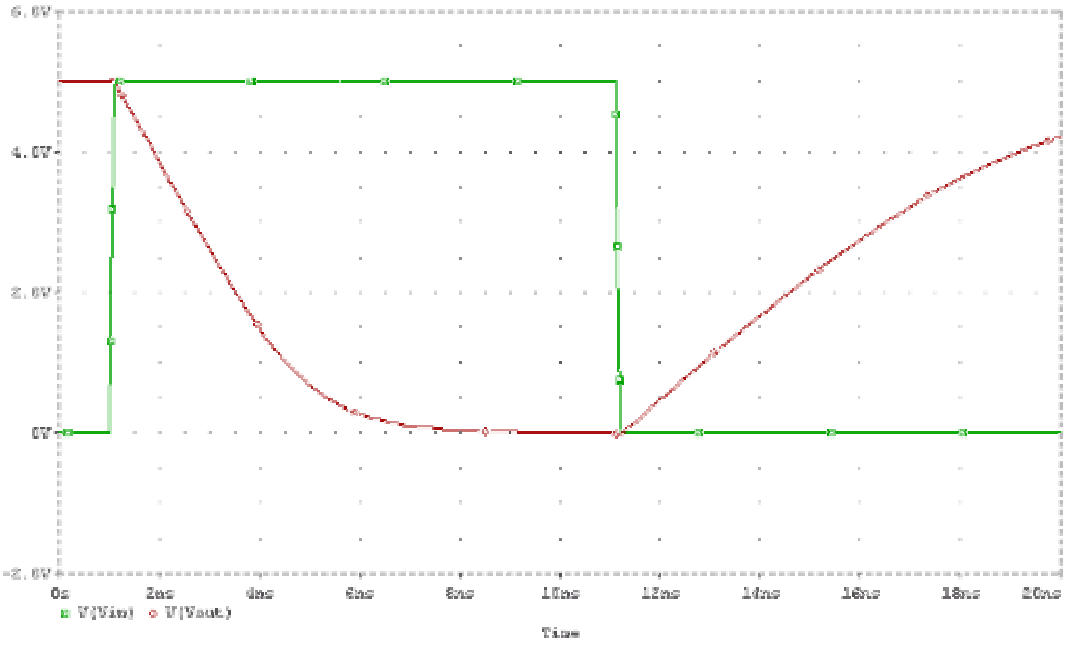


Problem 11.2

With W=10μm and a load capacitance of 1pF, C_{tot} = 1pF+2×10 ×2 ×800aF = 1.032pF. Rn1=12KΩ×2/10=2.4KΩ, Rp2=7.2KΩ. The propagation delay times are

t_{PHL}=2.4kΩ×1.032pF ≈ 2.5ns , t_{PLH}=7.2kΩ×1.032pF ≈ 7.43ns

Vin is Vpulse, whose parameters are: 0 5 1ns 0 0 10ns 20ns (not unique, you can use whatever proper parameters for the Vin)



Problem 11.3

For minimum size inverter, $t_{PHL}+t_{PLH}= 160k \times C_{ox} = 160k\Omega \times 4.8fF = 768ps$. Using 31 inverters, the oscillation frquency is

fosc = 1/(31×768ps) ≈ 42MHz.

Problem 12.1

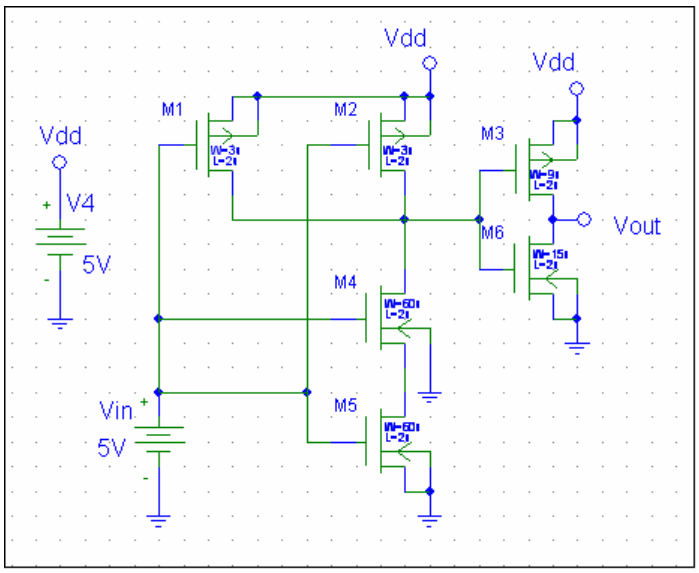
Solution: a) Design and hand-cal: The 2-input CMOS AND gate circuit diagram is shown below which consists of two parts NAND and INVERTOR cascaded:

To find Vsp, tie input A and B together as Vin. From NAND gate part, ignoring the body effect, we have

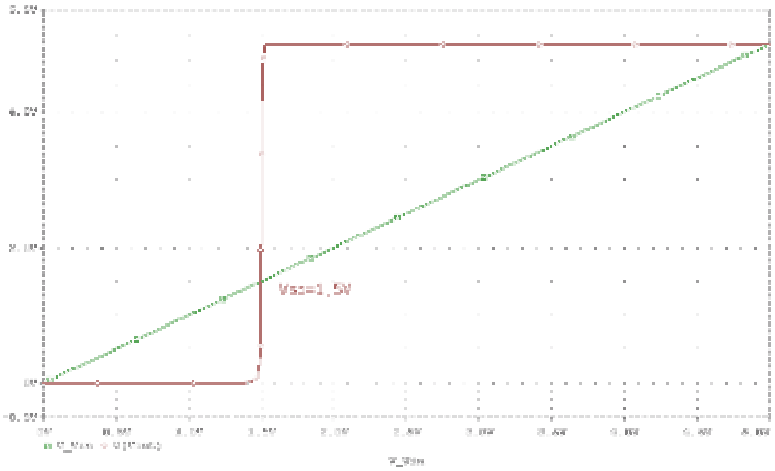
$$Vc = Vin = Vsp = \frac{\sqrt{\frac{\beta n}{4\beta p}}Vthn + (Vdd - Vthp)}{1+\sqrt{\frac{\beta n}{4\beta p}}} \qquad (12.1a)$$

$$Vout = Vc = Vsp = \frac{\sqrt{\frac{\beta n}{\beta p}}Vthn + (Vdd - Vthp)}{1+\sqrt{\frac{\beta n}{\beta p}}} \qquad (12.1b)$$

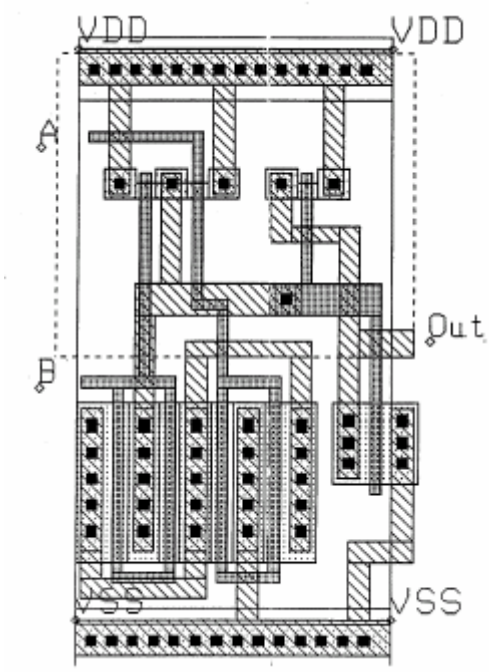
Vthn=0.83V, Vthp=0.91V, chosing all the length of CMOS L=2u, all Wp=3u for p-channel. Let both Vsp expression equals to 1.5 V, ==>> W4=W5=60u, W6=15u.



Again, While doing simulation to observe Vsp, let Va=Vb=Vin, and DC sweep Vin.



LAYOUT:



Problem 12.3

Solution: For N-input NOR gate, we have:

$$t_{PLH} = NRp(Coutp/N + NCoutn + Cload) + 0.35RpCinp(N-1)^2 \quad (12.3a)$$

$$t_{PHL} = (Rn/N)(NCoutn + Coutp/N + Cload) \quad (12.3b)$$

With minimum size MOSFEF, Rn=8kΩ, Rp=24kΩ, Coutn=Coutp=4.8fF, Cinp=7.2fF. and 3input.

a) With Cload=0:

$$t_{PLH} = 3x24k(4.8f/3 + 3x4.8f + 0) + 0.35x24kx7.2f(3-1)^2 = 1.394ns$$

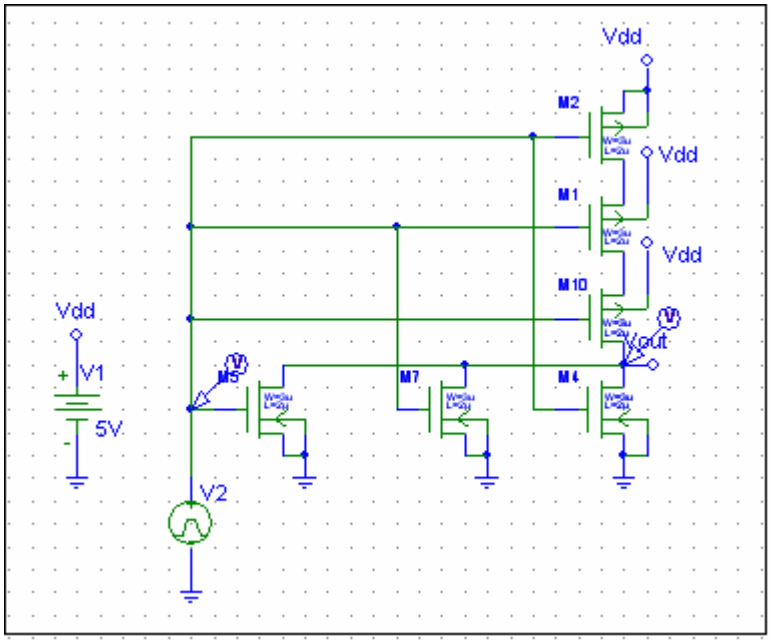
$$t_{PHL} = (8k/3)(3x4.8f + 4.8f/3 + 0) = 42.67ps$$

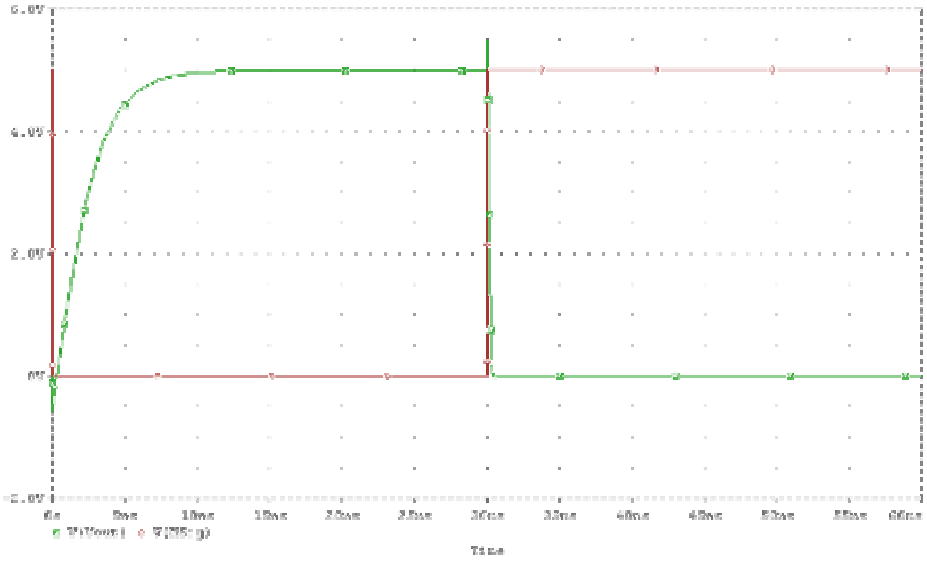
b) With Cload=100fF:

$$t_{PLH} = 3x24k(4.8f/3 + 3x4.8f + 100) + 0.35x24kx7.2f(3-1)^2 = 8.594ns$$

$$t_{PHL} = (8k/3)(3x4.8f + 4.8f/3 + 100) = 309ps$$

It can be seen that for 3-input NOR gate, the $t_{PLH} > t_{PHL}$, while for 3-input NAND gate, the $t_{PLH} < t_{PHL}$, also that the maximum delay time of NOR is bigger than the maximum delay time of NAND. Plus we already know that NAND gate has better Vsp and better noise margins. That is why in CMOS digital design, the NAND gate is used most often.





From the above Figure, tPLH=5ns. Zoom this result (see below), tPHL=160ps