Rules for Submitting the Assignment
This assignment must be submitted through blackboard, with the Subject "Home Work 3".

1. Which of the following is true of a device driver?
   (a) It is a part of the application software  
   (b) It is a part of the systems software  
   (c) It is a part of the device controller  
   (d) It is a part of the device itself  
   (e) It is a part of the driver hardware

2. Which of the following set of instructions is likely to be present at the kernel mode ISA, but not at the user mode ISA?
   (a) IN and OUT (read from or write to an I/O interface module register)  
   (b) CALL and RETURN (call or return from a subroutine)  
   (c) ADD and SUB (arithmetic instructions)  
   (d) SYSCALL (system call instruction)  
   (e) JMP and JZ (Unconditional and conditional jump instructions)  
   (f) None of the above.

3. A DMA (direct memory access) operation is
   (a) initiated and carried out by main memory  
   (b) initiated by the main memory, but carried out by the DMA controller  
   (c) initiated by the DMA controller, but carried out by the main memory  
   (d) initiated and carried out by the DMA controller  
   (e) initiated and carried out by the device driver  
   (f) initiated by the device driver, but carried out by the DMA controller  
   (g) initiated by the device driver, but carried out by the main memory

4. Which of the following functions/modules is unlikely to be entered when the user-level program calls the function scanf()?
   (a) read()  
   (b) system call interface  
   (c) file system  
   (d) process control system  
   (e) keyboard device driver

5. Which of the following functions/modules is unlikely to be used to read from the keyboard?
   (a) program-controlled IO  
   (b) interrupt-driven IO  
   (c) DMA  
   (d) IO processor

6. Which of the following is the most likely reason for disabling interrupts when entering the system call interface routine?
   (a) Once we are in the system call interface routine, no more interrupts/syscalls/exceptions are likely to occur.  
   (b) Most architectures have only one interrupt pin.  
   (c) Some book-keeping work (saving registers, etc) is required to be completed before the system can accept another interrupt.  
   (d) None of the above.
7. A DMA controller has a 32-bit status register and three 32-bit data registers. The status register is assigned to consecutive memory locations starting at label `DMA_status`. The three data registers are assigned to consecutive memory locations starting at label `DMA_data`. The controller interface works as follows. The controller is ready to accept a new command, only if the most significant bit (MSB) of its status register has been set to 1. When a new command is to be given to the DMA controller, the *DMA initiation device driver* writes the starting memory address in the first data register, the sector number in the second data register, and the number of bytes to be transferred in the third data register. After updating the data registers, the device driver sets the MSB of the status register to 0, and the next significant bit to 0 or 1 (0 for reading from IO device, and 1 for writing to IO device).

Write a MIPS-I assembly language device driver that can be used to initiate a DMA operation. This device driver is called with 4 parameters: `$a0$` contains the operations (0 for read; 1 for write); `$a1$` contains the starting address in memory; `$a2$` contains the sector number in the disk; and `$a3$` contains the number of bytes to be transferred. Assume that the return address is present in `$ra$`. 
