Q1. Design a 10-bit group ripple carry adder (GRCA) that uses 5-bit look ahead carry adder. Draw the logic diagram and write all Boolean equations for implementing such an adder. If the maximum fan in (i.e. number of inputs) allowed for a gate is 3, what is the worst-case delay of your adder?

Q2. Design a full subtractor module in a manner similar to the design of a full adder, and connect these modules to form an N-bit subtractor, in a manner similar to the design of an N-bit ripple carry adder. What is the worst-case delay of your subtractor?

Q3. Consider the data-path that appears in Midterm-2. For both the sw instruction, and beq instruction introduce control signals into your modified data-path. Translate the micro-routines you wrote in the answer to that question into control signal sequences.

Q4. What is the difference between Static RAM and Dynamic RAM? Which type of RAM is used to build main memory? Why?

Q5. Consider the data path given in figure 8.28 of the book. Write the MAL code for lw and add instructions. Specify the control signals that need to be asserted at each step. Also, draw the control signal timing for interpreting each of the microinstructions. Why is the timing important?

Q6. What is the role of tri-state buffers in a bus based data-path?