4.8 In the saturation mode also, \( i_D \) is directly proportional to \( W \). So, if \( W \) is halved, then \( i_D \) would also be halved. The vertical axis should therefore be scaled by 0.5.

For \( V_{OV} = 1.5V \), by looking at the corresponding curve, we observe that \( i_D = 0.5625 \text{ mA} \).

4.15 The NMOS transistor is operating in the linear resistance region (within the triode region), for which:

\[
i_D = k'_n \frac{W}{L} (v_{GS} - V_t)v_{DS}
\]

When \( v_{DS} = 0.1V \), for \( v_{GS} = 2V \), \( i_D = 60 \mu A \), and for \( v_{GS} = 4V \), \( i_D = 160 \mu A \).

\[
\frac{60\mu A}{160\mu A} = \frac{(2V - V_t) \times 0.1V}{(4V - V_t) \times 0.1V} \implies V_t = 0.8V
\]

Substituting \( V_t = 0.8 \text{ V} \) in the above equation, we get \( W/L = 10 \).

Substituting \( v_{GS} = 3 \text{ V} \), \( v_{DS} = 0.15 \text{ V} \), and \( k'_n = 50 \mu A/V^2 \) in the above equation, we get \( i_D = 0.165 \text{ mA} \).

In the pinch-off region, \( v_{DS} = v_{GS} - V_t = 3 \text{ V} - 0.8 \text{ V} = 2.2 \text{ V} \).

\[
i_D = k'_n \frac{W}{L} ((v_{GS} - V_t)v_{DS} - 0.5v_{DS}^2) = 1.21 \text{ mA}
\]

4.38 All three transistors are in saturation, as their drains are connected to their respective gates, guaranteeing that the individual \( v_{DSS} \)s \( > \) their \( v_{GS} - V_t \)s. While in saturation, the drain current is given by:

\[
i_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 \implies W = \frac{2i_D L}{k'_n (V_{GS} - V_t)^2}
\]

Transistor Q1: \( V_{GS} = 1.5 \text{ V} \implies W = 8 \mu \text{m} \)

Transistor Q2: \( V_{GS} = 2 \text{ V} \implies W = 2 \mu \text{m} \)

Transistor Q3: \( V_{GS} = 1.5 \text{ V} \implies W = 8 \mu \text{m} \)

4.49 a Point A: \( V_{IA} = V_t = 1 \text{ V} \); \( V_{OA} = V_{DD} = 5 \text{ V} \).

Point B: This is the boundary between the saturation and triode regions.

i.e., \( V_{OB} = V_{IB} - V_t \).

Also, \( I_{DB} = \frac{1}{2} k'_n \frac{W}{L} (V_{IB} - V_t)^2 \).

\( I_{DB} \) is also given by \( I_{DB} = \frac{V_{OB} - V_{OB}}{R_G} \).

Solving these two equations together, we get \( V_{OB} = 0.605 \text{ V} \) or \(-0.688 \text{ V} \), of which only the former one can be correct. Thus, \( V_{OB} = 0.605 \text{ V} \).

Then, \( V_{IB} = V_{OB} + V_t = 0.605 \text{ V} + 1 \text{ V} = 1.605 \text{ V} \).
b. \( V_{OVQ} = 0.5 \, \text{V} \implies V_{IQ} = V_{OVQ} + V_I = 0.5 \, \text{V} + 1 \, \text{V} = 1.5 \, \text{V} \).

\[ I_{DQ} = \frac{1}{2} k_n' \frac{W}{L} (V_{IQ} - V_I)^2 = 0.125 \, \text{mA} \]

\[ V_{OQ} = V_{DD} - I_{DQ} R_D = 2 \, \text{V}. \]

Incremental gain at bias point, \( A_v = \frac{R_D k_n' \frac{W}{L}}{2mA} \approx 12 \, \text{V/V} \).

c. The MOSFET will be in saturation for \( V_I \) ranging from 1 V to 1.605 V. If the bias point input is 1.5 V, it allows for only a 0.105 V input sine wave.

The amplitude of the output voltage signal that results is approximately equal to \( V_{OQ} - V_{OB} = 2 \, \text{V} - 0.605 \, \text{V} = 1.39 \, \text{V} \).

Gain = \( \frac{\text{Output amplitude}}{\text{Input amplitude}} = \frac{1.39V}{0.105V} = 13.29 \, \text{V/V} \).

This gain is \( \frac{13.29 - 12}{12} = 10.75\% \) more than the incremental gain calculated in part (b). This difference is because the segment of the voltage transfer curve considered here is not perfectly linear.

4.55 We plan to design the biasing circuit such that the transistor is in saturation mode.

We shall design \( R_D \) and \( R_S \) such that roughly one-third of the voltage drop (i.e., 15 V / 3 = 5 V) occurs across each of these resistors. Then

\[ R_D = R_S = \frac{5V}{2mA} = 2.5K\Omega \]

In saturation mode, \( I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_I)^2 \)

Substituting \( I_D = 2 \, \text{mA} \), \( k_n' = 80 \, \mu A/V^2 \), \( W/L = 40 \), and \( V_I = 1.2 \, \text{V} \) in this equation, we get \( V_{GS} = 2.32 \, \text{V} \) or 0.487 V, of which only the former is correct.

Thus, \( V_{GS} = 2.32 \, \text{V} \).

Voltage at the gate, \( V_G = V_S + V_{GS} = I_D R_S + V_{GS} = 2mA \cdot 2.5K\Omega + 2.32V = 7.32V \).

From the figure, we can see that \( V_G \) is obtained by the \( R_{G1} - R_{G2} \) voltage divider arrangement.

And, because the gate current is zero,

\[ V_G = 15V \frac{R_{G2}}{R_{G1} + R_{G2}} \]

As \( V_G = 7.32 \, \text{V} \) is less than \( 15 \, \text{V} / 2 \), \( R_{G2} < R_{G1} \). Therefore, \( R_{G1} = 22M\Omega \).

Substituting in the above equation, we get \( R_{G2} = 20.97M\Omega \).

With this biasing arrangement, \( V_{DS} = 5 \, \text{V} \). If it is designed to be at the edge of saturation, \( V_{DS} = V_{GS} - V_I = 2.32 \, \text{V} - 1.2 \, \text{V} = 1.12 \, \text{V} \), which is 5 V - 1.12 V = 3.88 V away from the edge of saturation.

4.68 In saturation mode, \( I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{OV})^2 = 0.5 \times 2mA/V^2 \times 1V^2 = 1mA \)

When a +0.1 V signal is superimposed on \( V_{GS} \), \( i_d = 0.5 \times 2mA/V^2 \times 1.1^2 = 1.21mA \)

Increment in drain current, \( i_d = 1.21mA - 1mA = 0.21mA \).
When a $-0.1 \text{ V}$ signal is superimposed on $V_{GS}$, $i_D = 0.5 \times 2mA/V^2 \times 0.9^2 = 0.81mA$

Decrement in drain current, $i_d = 1mA - 0.81mA = 0.19mA$

$$g_m \approx \frac{i_D}{V_{GS}} = \frac{0.21mA + 0.19mA}{0.1V + 0.1V} = \frac{0.4mA}{0.2V} = 2mA/V$$

From Equation 4.62, $g_m = k_n \frac{W}{L} V_O = 2mA/V$

The $g_m$ values are the same in both cases.

4.75 Because the gate current is zero, $V_G = V_D$. Therefore, the transistor is in saturation.

$$r_o = \frac{V_A}{I_D} = \frac{50V}{0.5mA} = 100K\Omega$$

$$V_G = V_D = 2V$$

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 0.5mA}{2V - 0.9V} = 0.91mA/V$$

Voltage gain, $\frac{v_o}{v_i} = -g_m(r_o || R_L) = -0.91mA/V (100K\Omega || 10K\Omega) = -8.3V/V$

When $I$ is increased to $1 \text{ mA}$, $V_{GS}$ can be calculated to be $2.5V$.

Therefore, $V_D = V_{GS} = 2.5 \text{ V}$.

New $r_o = \frac{50V}{1mA} = 50K\Omega$.

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2 \times 1mA}{2.5V - 0.9V} = 1.3mA/V$$

Voltage gain, $\frac{v_o}{v_i} = -g_m(r_o || R_L) = -1.3mA/V (50K\Omega || 10K\Omega) = -10.8V/V$