

GANG QU

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Notarization. I have read the following and certify that this curriculum vitae is a current and accurate statement of my professional record.

Signature _____

Date _____

1. Personal Information

Born in 1969 in Beijing, P.R.China.

Current Position: Assistant Professor, Electrical and Computer Engineering Department and
Institute for Advanced Computer Studies.

Affiliated with the Department of Computer Science.

Appointed to current position on August 16, 2000.

a. Education

- 2000 Ph.D. Computer Science, University of California, Los Angeles, California.
Dissertation: “*Constraint-Based Intellectual Property Protection: Theory and Practice*”.
- 1998 M.S. Computer Science, University of California, Los Angeles, California.
Thesis: “*Scheduling Problems for Reducing Energy on Variable Voltage Systems*” (**Outstanding Master of Science Award**).
- 1996 M.A. Mathematics, University of Oklahoma, Norman, Oklahoma.
- 1994 M.S. Applied Mathematics, University of Science and Technology of China, Hefei, Anhui, P.R.China.
- 1992 B.S. Pure Mathematics (major) and Non-linear Science (minor), University of Science and Technology of China, Hefei, Anhui, P.R.China. (**Outstanding Bachelor of Science Award**).

b. Honors and Awards

- September 2002 George Corcoran Award for teaching and educational leadership. University of Maryland, College Park. (also listed in section 3.c)
- August 2001 Best Student Paper Awards, *ACM SIGMOBILE International Conference on Mobile Computing and Networking*.
- April 2001 Individual Member of Virtual Socket Interface (VSI) Alliance.
- June 1999 Dimitris N. Chorafas Foundation Award.

- June 1999 36th ACM/IEEE Design Automation Conference Graduate Scholarship Award.
- January 1999 NCR Fellowship, National Cash Register Company.
- June 1998 Outstanding Master of Science Award, School of Engineering and Applied Science, University of California, Los Angeles, California.
- July 1992 Outstanding Bachelor of Science Award, University of Science and Technology of China, Hefei, Anhui, P.R.China.
- Member: IEEE, ACM SIGDA.

Students' Honors and Awards

- December 2004 Runner-up of the CRA outstanding undergraduate awards. Computer Research Associates. (**Jane Lin**)
- June 2004 Ph.D. forum. ACM/IEEE Design Automation Conference. (**Shaoxiong Hua**)
- August 2003 Best Project Award, Maryland Engineering Research Internship Teams (MERIT) program, University of Maryland, College Park, Maryland. (**Jane Lin** and **Matt Schmidt**)
- June 2003 University Booth. ACM/IEEE Design Automation Conference. (**Adarsh Jain, Lin Yuan, and Pushkin Pari**)
- August 2001 Best Presentation Award. MERIT program, University of Maryland, College Park, Maryland. (**Ming Liu** and **Ani Akinbiyi**)

c. Professional Experience

- August 2000 – present **Assistant Professor**
Electrical and Computer Engineering Department, University of Maryland, College Park, Maryland.
- January 2000 – June 2000 **Teaching Assistant**
Department of Computer Science, University of California, Los Angeles, California.
- July 1999 – October 1999 **Visiting Researcher**
Semiconductor Company of Toshiba Corporation, Kawasaki, Japan.
- July 1998 – June 1999 **Research Assistant**
Department of Computer Science, University of California, Los Angeles, California.
- September 1997 – June 1998 **Teaching Assistant**
Department of East Asia Languages and Cultures, University of California, Los Angeles, California.
- June 1997 – August 1997 **Software Engineer**
FEM Engineering Inc., Los Angeles, California.
- August 1994 – August 1996 **Teaching Assistant**
Department of Mathematics, University of Oklahoma, Norman, Oklahoma.
- September 1993 – July 1994 **Teaching Assistant**
Department of Mathematics, University of Science and Technology of China, Hefei, Anhui, P.R.China.

2. Research, Scholarly, and Creative Activities

[A]: co-authored with my Ph.D. advisor (M. Potkonjak) and his students; [S]: co-authored with my students; [C]: co-authored with my colleagues and my/their students; [Q]: single-authored by myself. All student names are underlined.

a. Books

A.1. G. Qu and M. Potkonjak, *Intellectual Property Protection in VLSI Designs: Theory and Practice*, Kluwer Academic Publishers, ISBN 1-4020-7320-8, January 2003. [A]

b. Chapters in Books

B.1. L. Yuan and G. Qu, “Energy Efficient Design for Secure Sensor Networks”, in *Handbook of Sensor Networks* (Chapter 38), CRC Press, ISBN 0-8493-1968-4, October 2004. [S]

c. Articles in Refereed Journals

13 published or accepted for publication. 9 in *IEEE transactions* (5 in *TCAD* and 3 in *TVLSI*), 3 in *ACM transactions and journals* (2 in *TECS*), and 1 in a *World of Science journal*.

C.1. I. Hong, D. Kirovski, G. Qu, M. Potkonjak, and M. Srivastava. “Power Optimization of Variable Voltage Core-Based Systems”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 12, pp. 1702–1714, December 1999. [A]

C.2. G. Qu, N. Kawabe, K. Usami, and M. Potkonjak. “Code Coverage-based Power Estimation Techniques for Microprocessors”, *Journal of Circuits, Systems, and Computers*, Vol. 11, No. 5, pp. 557–574, July 2002. [A]

C.3. S. Megerian, F. Koushanfar, G. Qu, G. Veltri, and M. Potkonjak. “Exposure In Wireless Sensor Networks: Theory and Practical Solutions”, *ACM Journal of Wireless Networks*, Kluwer Academic Publishers, Vol. 8, No. 5, pp. 443–454, September 2002. **(Invited as the best student paper awards winner from MobiCom 2001)** [A]

C.4. G. Qu and M. Potkonjak. “Techniques for Energy-Efficient Communication Pipeline Design”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 5, pp. 542–549, October 2002. [A]

C.5. G. Qu. “Publicly Detectable Watermarking for Intellectual Property Authentication in VLSI Design”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, No. 11, pp. 1363–1368, November 2002. [Q]

C.6. G. Qu and M. Potkonjak. “System Synthesis of Synchronous Multimedia Applications”, *ACM Transactions in Embedded Computing Systems (Special Issue on Memory Systems)*, Vol. 2, No. 1, pp. 74–97, February 2003. [A]

C.7. S. Hua and G. Qu. “QoP-Driven Scheduling for MPEG Video Decoding”, *IEEE Transactions on Consumer Electronics*, Vol. 49, No. 4, pp. 1341–1347, November 2003. **(Selected among the best papers from ICCE 2003)** [S]

C.8. J.L. Wong, G. Qu, and M. Potkonjak. “Optimization-Intensive Watermarking Techniques for Decision Problems”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 1, pp. 119–127, January 2004. [A]

C.9. A.E. Caldwell, H. Choi, A.B. Kahng, S. Mantik, M. Potkonjak, G. Qu, and J.L. Wong. “Effective Iterative Techniques for Fingerprinting Design IP”, *IEEE Transactions on*

Computer-Aided Design of Integrated Circuits and Systems, Vol. 23, No. 2, pp. 208–215, February 2004. [A]

C.10. J.L. Wong, G. Qu, and M. Potkonjak. “Power Minimization in QoS Sensitive Systems”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 6, pp. 553–561, June 2004. [A]

C.11. S. Hua and G. Qu. “Voltage Set-up Problem for Embedded Systems with Multiple Voltages”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 13, No. 7, July 2005 (accepted for publication, notified in January 2005, 4 pages). [S]

C.12. L. Yuan and G. Qu. “Analysis of Energy Reduction on Dynamic Voltage Scaling-Enabled Systems”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (accepted for publication, notified in January 2005, 10 pages). [S]

C.13. S. Hua, G. Qu, and S.S. Bhattacharyya. “Energy-Efficient Multi-Processor Implementation of Embedded Software”, *ACM Transactions in Embedded Computing Systems (Special Issue on Concurrent Hardware-Software Design Method for Multi-Processor System-On-Chip)*, (accepted for publication, notified in June 2005, 18 pages). [C]

d. Articles in Referred Journal under Revision/Review

D.1. S. Hua, G. Qu, and S.S. Bhattacharyya. “Probabilistic Design of Multimedia Embedded Systems”, *ACM Transactions in Embedded Computing Systems*. (submitted: December 2003, 2nd minor revision under review, 38 pages). [C]

D.2. S. Hua and G. Qu. “On Transferring Multimedia Application’s Tolerance to Execution Failure to Energy Reduction”, *IEEE Design and Test* (submitted: December 2003, 1st revision under preparation, 12 pages). [S]

D.3. S.N. Pamnani, D.N. Agarwal, G. Qu, and D. Yeung. “Low Power System Design with Performance Enhancement Techniques”, *Journal of Circuits, Systems, and Computers*. (submitted: December 2004, 1st revision under preparation, 20 pages). [C]

D.4. L. Yuan and G. Qu. “A Combined Gate Replacement and Input Vector Control Approach for Leakage Current Reduction”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (submitted: May 2005, 28 pages). [S]

e. Articles in Conference, Symposium, and Workshop Proceedings

54 papers have been published or accepted for publication. 35 are in highly competitive referred conferences, 16 are in other referred conferences, and 3 are in workshops without proceedings.

Highly competitive conferences, symposiums, and workshops

The following papers are published in the referred proceedings of the top 2~3 conferences in each technical field or conferences with acceptance rate below 35%. For conferences that accept full papers, short papers, and/or poster papers, the acceptance rate applicable to my paper is given.

E.1. I. Hong, D. Kirovski, G. Qu, M. Potkonjak, and M. Srivastava. “Power Optimization of Variable Voltage Core-Based Systems”, *35th ACM/IEEE Design Automation Conference Proceedings (DAC’98)*, pp. 176–181, June 1998. (acceptance rate: **36.4%**) [A]

- E.2. G. Qu and M. Potkonjak. “Techniques for Energy Minimization of Communication Pipelines”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’98)*, pp. 597–600, November 1998. (acceptance rate: **29.6%**) [A]
- E.3. G. Qu and M. Potkonjak. “Analysis of Watermarking Techniques for Graph Coloring Problem”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’98)*, pp. 190–193, November 1998. (acceptance rate: **29.6%**) [A]
- E.4. I. Hong, G. Qu, M. Potkonjak, and M.B. Srivastava. “Synthesis Techniques for Low-Power Hard Real-Time Systems on Variable Voltage Processor”, *19th IEEE Real-Time Systems Symposium (RTSS’98)*, pp. 178–187, December 1998. [A]
- E.5. A.E. Caldwell, H. Choi, A.B. Kahng, S. Mantik, M. Potkonjak, G. Qu, and J.L. Wong. “Effective Iterative Techniques for Fingerprinting Design IP”, *36th ACM/IEEE Design Automation Conference (DAC’99)*, pp. 843–848, June 1999. (acceptance rate: **34.1%**) [A]
- E.6. G. Qu, J.L. Wong, and M. Potkonjak. “Optimization-Intensive Watermarking Techniques for Decision Problems”, *36th ACM/IEEE Design Automation Conference (DAC’99)*, pp. 33–36, June 1999. (acceptance rate: **34.1%**) [A]
- E.7. G. Qu and M. Potkonjak. “Power Minimization Using System-Level Partitioning of Applications with Quality of Service Requirements”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’99)*, pp. 343–346, November 1999. (acceptance rate: **32.1%**) [A]
- E.8. Y. Chen, A.B. Kahng, G. Qu, and A. Zelikovsky. “The Associative-Skew Clock Routing Problem”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’99)*, pp. 168–171, November 1999. (acceptance rate: **32.1%**) [C]
- E.9. G. Qu, M. Mesarina, and M. Potkonjak. “System Synthesis of Synchronous Multimedia Applications”, *12th IEEE/ACM International Symposium on System Synthesis (ISSS’99)*, pp. 128–133, November 1999. (acceptance rate: **27.3%**) [A]
- E.10. G. Qu and M. Potkonjak. “Fingerprinting Intellectual Property Using Constraint-Addition”, *37th ACM/IEEE Design Automation Conference (DAC’00)*, pp. 587–592, June 2000. (acceptance rate: **34.6%**) [A]
- E.11. G. Qu, N. Kawabe, K. Usami, and M. Potkonjak. “Function-Level Power Estimation Methodology for Microprocessors”, *37th ACM/IEEE Design Automation Conference (DAC’00)*, pp. 810–813, June 2000. (acceptance rate: **34.6%**) [A]
- E.12. G. Qu and M. Potkonjak. “Energy Minimization with Guaranteed Quality of Service”, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED’00)*, pp. 43–48, July 2000. (acceptance rate: **24.1%**) [A]
- E.13. G. Qu and M. Potkonjak. “Achieving Utility Arbitrarily Close to Optimal with Limited Energy”, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED’00)*, pp. 125–130, July 2000. (acceptance rate: **24.1%**) [A]
- E.14. F. Koushanfar, G. Qu, and M. Potkonjak. “Intellectual Property Metering”, *4th Information Hiding Workshop (IHW’01)*, pp. 87–102, LNCS Vol. 2137, Springer-Verlag, April 2001. [A]
- E.15. G. Qu. “Keyless Public Watermarking for Intellectual Property Authentication”, *4th Information Hiding Workshop (IHW’01)*, pp. 103–118, LNCS Vol. 2137, Springer-Verlag, April 2001. [Q]
- E.16. F. Koushanfar and G. Qu. “Hardware Metering”, *38th ACM/IEEE Design Automation Conference (DAC’01)*, pp. 490–493, June 2001. [C]

- E.17. G. Qu. “Publicly Detectable Techniques for the Protection of Virtual Components”, *38th ACM/IEEE Design Automation Conference (DAC’01)*, pp. 474–479, June 2001. [Q]
- E.18. S. Meguerdichian, F. Koushanfar, G. Qu, and M. Potkonjak. “Exposure in Wireless Ad-hoc Sensor Networks”, *ACM SIGMOBILE International Conference on Mobile Computing and Networking (MobiCom’01)*, pp. 139–150, July 2001. (Best Student Paper Award) [A]
- E.19. G. Qu. “What is the Limit of Energy Saving by Dynamic Voltage Scaling?” *IEEE/ACM International Conference on Computer Aided Design (ICCAD’01)*, pp. 560–563, November 2001. (acceptance rate: **30.6%**) [Q]
- E.20. J.L. Wong, G. Qu, and M. Potkonjak. “An On-line Approach for Power Minimization in QoS Sensitive Systems”, *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC’03)*, pp. 59–64, January 2003. (acceptance rate: **33.6%**) [A]
- E.21. A. Jain, L. Yuan, P. Pari, and G. Qu. “Zero Overhead Watermarking Technique for FPGA Designs”, *13th IEEE /ACM Great Lakes Symposium on VLSI (GLSVLSI’03)*, pp. 147–152, April 2003. (acceptance rate: **12.5%**) [S]
- E.22. S. Hua, G. Qu, and S.S. Bhattacharyya. “Energy Reduction Techniques for Multimedia Applications with Tolerance to Deadline Misses”, *40th ACM/IEEE Design Automation Conference (DAC’03)*, pp. 131–136, June 2003. (acceptance rate: **24.2%**) [S]
- E.23. S. Hua, G. Qu, and S.S. Bhattacharyya. “Energy-Efficient Multi-Processor Implementation of Embedded Software”, *3rd ACM International Conference on Embedded Software (EMSOFT’03)*, pp. 257–273, October 2003. (acceptance rate: **33.3%**) [S]
- E.24. G. Veltri, Q. Huang, G. Qu, and M. Potkonjak. “Minimal and Maximal Exposure Path Algorithms for Wireless Embedded Sensor Networks”, *1st ACM Conference on Embedded Networked Sensor Systems (SenSys’03)*, pp. 40–50, November 2003. (acceptance rate: **17%**) [A]
- E.25. S. Hua and G. Qu. “Approaching the Maximum Energy Saving on Embedded Systems with Multiply Voltages”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’03)*, pp. 26–29, November 2003. (acceptance rate: **26.3%**) [S]
- E.26. S. Hua and G. Qu. “QoS-Driven Scheduling for Multimedia Applications”, *IEEE International Symposium on Circuits and Systems (ISCAS’04)*, Vol. 2, pp. 125–128, May 2004. (acceptance rate: **34.9%**) [S]
- E.27. D. Agarwal, S. Pamnani, G. Qu, and D. Yeung. “Transferring Performance Gain from Software Prefetching to Energy Reduction”, *IEEE International Symposium on Circuits and Systems (ISCAS’04)*, Vol. 2, pp. 241–244, May 2004. (acceptance rate: **34.9%**) [C]
- E.28. A. Balkan, G. Qu, and U. Vishkin. “Arbitrate-and-Move Primitives for High Throughput On-Chip Interconnection Networks”, *IEEE International Symposium on Circuits and Systems (ISCAS’04)*, Vol. 2, pp. 441–444, May 2004. (acceptance rate: **34.9%**) [C]
- E.29. P. Pari, L. Yuan, and G. Qu. “How Many Solutions Does a SAT Instance Have?”, *IEEE International Symposium on Circuits and Systems (ISCAS’04)*, Vol. 5, pp. 209–212, May 2004. (acceptance rate: **34.9%**) [S]
- E.30. L. Yuan and G. Qu. “Information Hiding in Finite State Machine”, *6th Information Hiding Workshop (IHW’04)*, pp. 340–354, LNCS Vol. 3200, Springer-Verlag, May 2004. (acceptance rate: **30%**) [S]
- E.31. L. Yuan, P. Pari, and G. Qu. “Soft IP Protection: Watermarking HDL Source Codes”, *6th Information Hiding Workshop (IHW’04)*, pp. 224–238, LNCS Vol. 3200, Springer-Verlag, May 2004. (acceptance rate: **30%**) [S]

- E.32. S. Hua and G. Qu. “Energy-Efficient Dual-Voltage Soft Real-Time System with (m,k)-Firm Deadline Guarantee”, *ACM International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES’04)*, pp. 116–123, September 2004.
(acceptance rate: **30.4%**) [S]
- E.33. L. Yuan, G. Qu, T. Villa, and A. Sangiovanni-Vincentelli. “FSM Re-Engineering and Its Application in Low Power State Encoding”, *IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC’05)*, pp. 254–259, January 2005. (acceptance rate: **14.3%**) [C]
- E.34. S. Hua and G. Qu. “Power Minimization Techniques on Distributed Real-Time Systems by Global and Local Slack Management”, *IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC’05)*, pp. 830–835, January 2005. (acceptance rate: **14.3%**) [S]
- E.35. L. Yuan and G. Qu. “Enhanced Leakage Reduction Technique by Gate Replacement”, *42nd ACM/IEEE Design Automation Conference (DAC’05)*, pp. 47–50, June 2005.
(acceptance rate: **20.9%**) [S]

Other referred conferences, symposiums, and workshops

- E.36. K.T. Kornegay, G. Qu, and M. Potkonjak. “Quality of Service and System Design”, *IEEE Computer Society Annual Workshop on VLSI, Theme: System Level Design (WVLSI’99)*, pp. 112–117, April 1999. (**invited**) [A]
- E.37. G. Qu, D. Kirovski, M. Potkonjak, and M.B. Srivastava. “Energy Minimization of System Pipelines Using Multiple Voltages”, *IEEE International Symposium on Circuits and Systems (ISCAS’99), VLSI, Vol. 1*, pp. 362–365, May 1999. (**invited**) [A]
- E.38. G. Qu and M. Potkonjak. “Hiding Signatures in Graph Coloring Solutions”, *3rd Information Hiding Workshop (IHW’99)*, pp. 391–408, September 1999. [A]
- E.39. G. Qu, J.L. Wong, and M. Potkonjak. “Fair Watermarking Techniques”, *IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC’00)*, pp. 55–60, January 2000. [A]
- E.40. L. Yuan and G. Qu. “Design Space Exploration for Energy-Efficient Secure Sensor Network”, *13th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP’02)*, pp. 88–97, July 2002. [S]
- E.41. S. Hua and G. Qu. “A New Quality of Service Metric for Hard/Soft Real-Time Applications”, *IEEE International Conference on Information Technology: Coding and Computing (ITCC’03)*, pp. 347–351, April 2003. [S]
- E.42. S. Hua, G. Qu, and S.S. Bhattacharyya. “Exploring the Probabilistic Design Space of Multimedia Systems”, *14th IEEE International Workshop on Rapid System Prototyping (RSP’03)*, pp. 233–240, June 2003. [S]
- E.43. S. Hua and G. Qu. “QoP-Driven Scheduling for MPEG Video Decoding”, *22nd IEEE International Conference on Consumer Electronics (ICCE’03)*, pp. 48–49, June 2003. [S]
- E.44. G. Qu. “Introducing the Concept of Design Reuse into Undergraduate Digital Design Curriculum”, *4th IEEE/ACM International Conference on Microelectronic Systems Education (MSE’03)*, pp. 10–11, June 2003. (**education related**) [Q]
- E.45. P. Pari, J. Lin, L. Yuan, and G. Qu. “Generating “Random” 3-SAT Instances with Specific Solution Space Structure”, *19th National Conference on Artificial Intelligence (AAAI) and 16th Innovative Applications of Artificial Intelligence Conference (IAAI)*, pp. 960–961, July 2004. (**abstract**) [S]

- E.46. L. Yuan, P. Pari, and G. Qu. “Finding Redundant Constraints for FSM Minimization”, *19th National Conference on Artificial Intelligence (AAAI) and 16th Innovative Applications of Artificial Intelligence Conference (IAAI)*, pp. 976–977, July 2004. **(abstract)** [S]
- E.47. J. Feng, G. Qu, and M. Potkonjak. “Differential On-line Sensor Calibration”, *3rd IEEE Conference on Sensors (Sensors2004)*, pp. 417–420, October 2004. [A]
- E.48. J. Feng, G. Qu, and M. Potkonjak. “Sensor Calibration using Nonparametric Statistical Characterization of Error Models”, *3rd IEEE Conference on Sensors (Sensors2004)*, pp. 1456–1459, October 2004. [A]
- E.49. L. Yuan, G. Qu, and A. Srivastava. “VLSI CAD Tool Protection by Birthmarking Design Solutions”, *15th IEEE /ACM Great Lakes Symposium on VLSI (GLSVLSI’05)*, pp. 341–344, April 2005. [S]
- E.50. V. Kianzad, S.S. Bhattacharyya, and G. Qu. “CASPER: An Integrated Energy-Driven Approach for Task Graph Scheduling on Distributed Embedded Systems”, *16th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP’05)*, July 2005. [C]
- E.51. S. Leventhal, L. Yuan, M.K. Bambha, S.S. Bhattacharyya, and G. Qu. “DSP Address Optimization Using Evolutionary Algorithms”, *9th International Workshop on Software and Compilers for Embedded Systems (SCOPE’05)*, September 2005. [C]

Non-refereed workshops (without proceedings)

- E.52. J. Wong, G. Qu, and M. Potkonjak. “Power Minimization under QoS Constraints”, *IEEE International Packetvideo Workshop*, April 2002. **(invited)** [A]
- E.53. S. Hua and G. Qu. “On-Line Voltage Scheduling for Multimedia Applications”, *1st Workshop on Embedded Systems for Real-Time Multimedia (ESTMedia’03)*, pp. 24–31, October 2003. [S]
- E.54. L. Yuan and G. Qu. “FSM Re-Engineering for Low Power State Encoding”, *13th International Workshop on Logic and Synthesis (IWLS’04)*, pp. 257–264, June 2004. [S]

f. Conference Presentations

- F.1. “Power Optimization of Variable Voltage Core-Based Systems”, *35th ACM/IEEE Design Automation Conference (DAC’98)*, San Francisco, California, June 17, 1998.
- F.2. “Analysis of Watermarking Techniques for Graph Coloring Problem”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’98)*, San Jose, California, November 9, 1998.
- F.3. “Techniques for Energy Minimization of Communication Pipelines”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’98)*, San Jose, California, November 11, 1998.
- F.4. “Quality of Service and System Design”, *IEEE Computer Society Annual Workshop on VLSI (WVLSI’99)*, Orlando, Florida, April 9, 1999.
- F.5. “Energy Minimization of System Pipelines Using Multiple Voltages”, *IEEE International Symposium on Circuits and Systems (ISCAS’99)*, Orlando, Florida, May 31, 1999.
- F.6. “Optimization-Intensive Watermarking Techniques for Decision Problems”, *36th ACM/IEEE Design Automation Conference (DAC’99)*, New Orleans, Louisiana, June 22, 1999.
- F.7. “System Design for Quality of Service Guarantees”, *IEEE/ACM International Conference on Computer Aided Design (ICCAD’99)*, San Jose, California, November 9, 1999.

- F.8. "System Synthesis of Synchronous Multimedia Applications", *12th IEEE/ACM International Symposium on System Synthesis (ISSS'99)*, San Jose, California, November 12, 1999.
- F.9. "Constraint Manipulation for Fingerprinting Intellectual Property", *37th ACM/IEEE Design Automation Conference (DAC'00)*, Los Angeles, California, June 7, 2000.
- F.10. "Function-Level Power Model and Estimation", *37th ACM/IEEE Design Automation Conference (DAC'00)*, Los Angeles, California, June 8, 2000.
- F.11. "IP Authentication – As Easy as Grandma Can Do", *4th Information Hiding Workshop (IHW'01)*, Pittsburgh, Pennsylvania, April 25, 2001.
- F.12. "Intellectual Property Metering", *4th Information Hiding Workshop (IHW'01)*, Pittsburgh, Pennsylvania, April 25, 2001.
- F.13. "Publicly Detectable Techniques for the Protection of Virtual Components", *38th ACM/IEEE Design Automation Conference (DAC'01)*, Las Vegas, Nevada, June 20, 2001.
- F.14. "What is the Limit of Energy Saving by Dynamic Voltage Scaling?" *IEEE/ACM International Conference on Computer Aided Design (ICCAD'01)*, San Jose, California, November 7, 2001.
- F.15. "Power Minimization under QoS Constraints via DVS", *IEEE International Packetvideo Workshop*, Pittsburgh, Pennsylvania, April 25, 2002.
- F.16. "Design of Energy-Efficient Secure Sensor Network", *13th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'02)*, San Jose, California, July 17, 2002.
- F.17. "Probabilistic Design of Multimedia Systems", *14th IEEE International Workshop on Rapid System Prototyping (RSP'03)*, San Diego, California, June 11, 2003.
- F.18. "QoP-Driven Scheduling for MPEG Video Decoding", *22nd IEEE International Conference on Consumer Electronics (ICCE'03)*, Los Angeles, California, June 17, 2003.
- F.19. "On-Line Voltage Scheduling for Low Power Probabilistic Design of Multimedia Systems", *1st Workshop on Embedded Systems for Real-Time Multimedia (ESTImedia'03)*, New Port Beach, California, October 3, 2003.
- F.20. "Energy-Efficient Multi-Processor Implementation of Embedded Software", *3rd ACM International Conference on Embedded Software (EMSOFT'03)*, Philadelphia, Pennsylvania, October 14, 2003.
- F.21. "Energy-Efficient Dual-Voltage Soft Real-Time System with (m,k)-Firm Deadline Guarantee", *ACM International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES'04)*, Washington, DC, September 23, 2004.
- F.22. "Power Minimization Techniques on Distributed Real-Time Systems by Global and Local Slack Management", *IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC'05)*, Shanghai, China, January 21, 2005.

g. Invited Talks

- G.1. "Power Estimation and Modeling for VLSI Circuits – State-of-the-Art Techniques", Semiconductor Company of Toshiba Corporation, Kawasaki, Japan, August 25, 1999.
- G.2. "Watermarking-Based Intellectual Property Protection", *Computer Science Department*, University of California, Los Angeles, California, February 15, 2000.

- G.3. “On Dynamic Voltage Scaling for Low Power Computing”, *ECE Faculty Seminar Series*, University of Maryland, College Park, Maryland, November 9, 2001.
- G.4. “Power Management of Multi-Processor Multi-Voltage Embedded Systems via Task Scheduling”, *Minta Martin Presentations*, University of Maryland, College Park, Maryland, June 21, 2002.
- G.5. “Security Issues in VLSI and Embedded System Design”, *2002 US-China Conference on Business and Technology*, Washington, DC, December 7, 2002.
- G.6. “Protecting VLSI Design IPs”, *Associate Dean’s Junior Faculty Seminar*, University of Maryland, College Park, Maryland, March 20, 2003.
- G.7. “Low Power Embedded System Design in the Nanometer Era”, Tsinghua University, Beijing, China, January 6, 2005.
- G.8. “New Advances in DVS for Low Power Embedded System Design”, IBM T.J. Watson Research Lab, April 29, 2005.

h. Panel, Tutorial, and Other Talks

- H.1. **(lecture)** “Security Issues in Intellectual Property Reuse and IP-Based Design”, *1st ACM SIGDA Design Automation Summer School*, Cape Cod, Massachusetts, May 26, 2001.
- H.2. **(panel)** “What Is Available in IPP and How Can You Profit from It?”, *IEEE International SOC Conference*, Portland, Oregon, September 18, 2003.
- H.3. **(tutorial)** “Intellectual Property Protection in Semiconductor and VLSI Design”, *IEEE/ACM Asia South Pacific Design Automation Conference*, Shanghai, China, January 18, 2005.

i. Contracts and Grants

I.1. National Science Foundation

MRI: Development of Energy-Efficient Embedded Systems for Wireless Sensor Networks. Co-Principal Investigator (PI: A. Ephremides. Other Co-PI and senior personnel: P. Abshire, R. Barua, B. Jacob, P. Petrov, and S. Ulukus). \$399,999, 2005–2010.

I.2. Microsoft Research

A Multidisciplinary and Integrated Approach to Raise the Global Awareness of Trustworthy Computing. Principal Investigator. \$50,000, 2005–2006.

I.3. National Science Foundation

ITR: PRAM on Chip. Co-Principal Investigator (PI: U. Vishkin. Other Co-PI and senior personnel: R. Barua, M. Franklin, B. Jacob, C. Tseng, and D. Yeung). \$750,000, 2004–2007.

I.4. ACM/IEEE Travel Grants

Design Automation Conference (DAC) by DAC and ACM SIGDA. \$1,000, 2001.

International Conference on Computer-Aided Design (ICCAD) by ICCAD and IEEE Circuit and Systems Society, \$1,150, 2001.

University of Maryland Internal

I.5. GRB Summer Research Award

Where Are the Hard SAT Instances. The General Research Board, University of Maryland, College Park. Principal Investigator. \$8,750, 2005.

I.6. International Travel Award

Intellectual Property Protection in Semiconductor Industry in China. Office of International Program, University of Maryland, College Park. Principal Investigator. \$1,350, 2005.

I.7. Minta Martin Research Fund.

Power Management of Multi-Processor Multi-Voltage Embedded System via Task Scheduling. Glenn L. Martin Institute of Technology, University of Maryland, College Park. Principal Investigator. \$55,000, 2001–2002.

Pending

I.8. National Science Foundation

Voltage Scaling Based Energy Efficient Multi-Processor Design of Soft Real-Time Embedded System. Principal Investigator. \$274,350, 2005–2008.

I.9. National Collegiate Inventors and Innovators Alliance

Secure E-Payment System. Principal Investigator. \$14,837, 2005–2006.

I.10. National Science Foundation

SIRG: Fundamental Energy Limits in Wireless Sensor Networks. Co- Principal Investigator (PI: A. Ephremides. Other Co-PI and senior personnel: P. Abshire, R. Barua, P. Petrov, and S. Ulukus). \$2,499,483, 2005–2010.

j. Citations

161 citations according to ACM Digital Library (<http://portal.acm.org/>)

259 citations according to CiteSeer: Scientific Literature Digital Library (<http://citeseer.ist.psu.edu/>)

564 citations according to Google Scholar (<http://scholar.google.com/>)

56 citations according to ISI Web of Science (<http://isi17.isiknowledge.com/portal.cgi/>)

3. Teaching, Mentoring, and Advising Activities

a. Courses Taught

I have taught ENEE 114 (3 times), ENEE 244 (3 times), ENEE 644 (3 times), and ENEE 759Q (1 time). The teaching evaluation is conducted by the students at the end of each semester. The maximum score is 4.00. The “Dept. Average” column is the average teaching evaluation of all courses of the same level offered by the department. ENEE 698B and ENEE 499 do not have teaching evaluation.

Semester	Course Number	Course Title	Enrollment	Teaching Evaluation	Dept. Average
Fall 2000	ENEE 244	Digital Logic Design	72	3.31	3.24
Spring 2001	ENEE 644	Computer-Aided Design of Digital Systems	56	3.33	3.30
	ENEE 698B	Computer Engineering Seminar	10	N/A	N/A
Summer 2001	ENEE 499	Undergraduate Research Project	2	N/A	N/A
Fall 2001	ENEE 244	Digital Logic Design	83	3.21	3.14
	ENEE 499	Undergraduate Research Project	1	N/A	N/A
Spring 2002	ENEE 644	Computer-Aided Design of Digital Systems	58	3.47	3.20
	ENEE 698B	Computer Engineering Seminar	21	N/A	N/A
Fall 2002	ENEE 759Q	Intellectual Property Protection: from Multimedia Data to Software and VLSI Design	14	3.90	3.24
Spring 2003	ENEE 644	Computer-Aided Design of Digital Systems	46	3.37	3.23
Summer 2002	ENEE 499	Undergraduate Research Project	1	N/A	N/A
Fall 2003	ENEE 244	Digital Logic Design	64	3.25	3.19
	ENEE 499	Undergraduate Research Project	1	N/A	N/A
Spring 2004	ENEE 114	Programming Concepts for Engineers	95	3.13	2.90
Fall 2004	ENEE 114	Programming Concepts for Engineers	53	3.04	3.10
Spring 2005	ENEE 114	Programming Concepts for Engineers	86	3.46	3.18
Fall 2005	ENEE 759B	Advances in Low Power Design Methodologies			
	ENEE 499	Undergraduate Research Project			

b. Course or Curriculum Development

- **New Courses**

ENEE 759Q: *Intellectual Property Protection: from Multimedia Data to Software and VLSI Design*

This course was introduced in Fall 2002. It covers the VLSI (very large scale integrated circuit) intellectual property (IP) reuse based design methodology, the industrial IP protection standards, software watermarking and obfuscation, multimedia watermarking, and basics on cryptography and steganography.

Besides ECE graduate students, this course has attracted students from the business school and ECE undergraduates. Out of the eight course projects, one was published in a competitive conference in Spring 2003 [E.21], two were later developed into conference papers in Spring 2004 [E.30 and E.31], one finished as a survey report, and one term paper attracted IBM's interest and the student got an Internship. One student accepted a position at the U.S. patent office shortly after the course was over.

ENEE 459B: *Introduction to Trustworthy Computing* (currently under preparation)

This course is partly supported by a grant from Microsoft Research (see section 2.i: Contracts and Grants) and will be offered in Spring 2006 for junior/senior undergraduates. It will cover the "four pillars" of trustworthy computing: (i) security, (ii) privacy, (iii) reliability, and (iv) business integrity. One of its unique features will be the integration of rich computer science and engineering content and case studies with business flavor. Course material will be made available to the public via Microsoft Developer Network Academic Alliance Curriculum Repository and the National Information Assurance Training and Education Center.

- **Significant Revisions**

ENEE 644: *Computer-Aided Design of Digital Systems*

This course previously covered both logic synthesis and system level design of VLSI computer-aided design (CAD). These topics are normally offered in peer schools as two separate graduate level courses. I revised it to focus on (i) the logic synthesis and optimization and (2) basic algorithms used in CAD tools when I first offered it in Spring 2001. The lecture notes were posted on the course web page. They have been adopted by other faculty who offered this course recently and referenced by other schools.

ENEE 698B: *Computer Engineering Seminar*

This 1-credit graduate seminar course requires students to read, present, and discuss technical papers and articles. I observed students' difficulties in presentation and thus developed a set of presentation-related questions (e.g., how to present the title page, how to use tables and figures, how to use animations, colors, and fonts, etc.). The students were asked to discuss these questions, judge each other's presentation, and write a report every week. As a result, most students taking this seminar have significantly improved their presentation skills. This has benefited them in their conference presentations and thesis defense. With the inclusion of an oral component in the new Ph.D. qualifying exam, this will be even more helpful.

ENEE 759B: *Advances in Low Power Design Methodologies*

This course was last offered in 1998. Since then, power and energy efficient design has gained more and more attention. The revision, which will be offered in Fall 2005, covers the fundamentals in low power design, and includes the new challenges, solutions, and applications

from the cutting-edge research and industrial practice. Similar to ENEE 759Q, this course will be research oriented. Conference papers/submissions, term papers, and scholarly papers that satisfy the M.S. degree requirement (non-thesis option) are expected.

- **Other**

ENEE 114: *exemption exam development*

Each semester, there are a number of transfer students who request to be exempted from taking this basic programming course. In the past, if the student has taken the course from an institution that is not in the ECE department's approved list, we needed to evaluate the student's request by checking the textbook(s) being used, course syllabus, homework, projects, exams, and student's grade. In Fall 2004, Dr. Judith Bell, the department's director for undergraduate studies, proposed to establish an exemption exam to make this process formal and consistent. I developed the exemption exam during the winter break of 2004–2005. One student took the exam, which was graded by myself, in the beginning of Spring 2005.

New Ph.D. qualifying exam: *digital logic design problem development*

Starting from Fall 2004, the ECE department offers incoming Ph.D. students a new format of Ph.D. qualifying exam (written). Dr. Shuvra Bhattacharyya has been in charge of the computer engineering part of the exam. I have been helping him to provide problems and answers for the *digital logic design* part based on course ENEE 244. The exam was given for the first time in Spring 2005 and the reaction was quite positive. I have also prepared a different set of exam problems and answers that will be given in Fall 2005.

Use of Information Technology

Comprehensive web pages have been designed and maintained for all the above courses. They include all the course materials: syllabus, homework assignments and solutions, sample exams, projects, lecture notes, important announcements, and related links. Lectures for these courses (except ENEE 114, Programming Concepts for Engineers) are delivered in PowerPoint presentations and posted on the web pages in PDF format. The lecture notes for ENEE 644 have been adopted in Spring 2004 and Spring 2005 when the course was taught by another professor. Part of it has also been referenced by other schools.

For ENEE 114, example programs are compiled and executed during the lecture and made available to the students through the course web page. Programming projects, quizzes, and small homework are collected electronically by the UNIX *submit* command.

Email has been heavily used for communication between students and the instructor.

For both undergraduate courses ENEE 114 and ENEE 244, a class survey was taken in the first half of the semester and adjustment has been made accordingly in the lecture and TA recitation. Each student's projected grade and the rank in the class are posted twice every semester, once in the middle of the semester and once before the final exam, to help student understand their positions in the class and the grades they could expect.

The ongoing work on ENEE 459B will be made available to the public via Microsoft Developer Network Academic Alliance Curriculum Repository (<http://www.msdnaa.net/curriculum>) and the National Information Assurance Training and Education Center (<http://niattec.info/>).

c. Teaching Awards and other Recognitions

- George Corcoran Award
“For significant contributions to electrical and computer engineering education. In recognition of teaching and educational leadership at the College Park campus. Effective contributions at the National Level and creative and other scholarly activities related to electrical and computer engineering education. University of Maryland, College Park, Maryland.” September 2002.
(also listed in section 1.b)
- Lecturer in the First ACM SIGDA Design Automation Summer School
“In Recognition of Qu, Gang for his contribution to the ACM SIGDA Design Automation Summer School.” May 2001.
- Education related publication
“Introducing the Concept of Design Reuse into Undergraduate Digital Design Curriculum”, *4th IEEE/ACM International Conference on Microelectronic Systems Education (MSE'03)*, pp. 10–11, June 2003.
(also listed as [E.44] in section 2.e)
- Involvement in education oriented conference
Technical Program Committee Member: *IEEE International Conference on Microelectronics Systems Education* (<http://www.mseconference.org>)
Reviewer: *ACM SIGCSE Technical Symposium on Computer Science Education* (<http://www.sigcse.org/>) (also listed in section 4.b)

d. Advising

I have graduated 1 Ph.D. student, 5 M.S. students (2 with thesis and 3 with scholarly paper). 1 Ph.D. student has passed his proposal defense and is expected to graduate in Spring 2006.

In addition, I have served on the committees for 12 Ph.D. students and 10 M.S. students.

▪ **Research Advising**

Ph.D. Theses

- Shaoxiong Hua (Fall 2001 – Spring 2004)
Thesis: *Providing QoS with Reduced Energy Consumption via Voltage Scaling on Embedded Systems*
Starting Employment: Synopsys
- Lin Yuan (Fall 2001 – Spring 2006 Expected)
Thesis: *Design Space Exploration in Embedded System Design and Implementation*
Proposal defense: Spring 2005

M.S. Theses

- Pushkin J. Pari (Spring 2002 – Spring 2004)
Thesis: *Several Issues on the Boolean Satisfiability (SAT) Problem*
Starting Employment: Intel

- Adarsh K. Jain (Fall 2001 – Summer 2003)
Thesis: *Achieving Zero Overhead Watermarking for FPGA Designs*
Starting Employment: CERN, European Organisation for Nuclear Research

M.S. Scholarly Paper (1st reader)

- Thomas J. Keeley (Spring 2004)
- Bei Wang (Spring 2003)
- Anusha Parisutham (Spring 2003)

Undergraduate Students

- Jane Lin (Summer 2003 – Fall 2004, MERIT Program)
Starting Employment: Booze Allen
- Timothy P. Burke (Summer 2005 – Spring 2006 Expected)
- Le Chang (Summer 2005 – Spring 2006 Expected)
- Matt Schmidt (Purdue University) (Summer 2002, 2003, MERIT Program)
- Chih-Yuan Huang (U.C. Berkeley) (Summer 2002, MERIT Program)
- Ani Akinbiyi (Summer 2001 – Fall 2001, MERIT Program)
- Ming Liu (Summer 2001, MERIT program)

▪ **Thesis Committee Service**

Ph.D. (proposal and/or thesis defense of 12 students)

Cagdas Dirik	(Advisor: Jacob	Proposal: Summer 2005, Thesis:)
Fuat Keceli	(Advisor: Vishkin	Proposal: Summer 2005, Thesis:)
Mainak Sen	(Advisor: Bhattacharyya	Proposal: Summer 2005, Thesis:)
Dong-Ik Ko	(Advisor: Bhattacharyya	Proposal: Fall 2004, Thesis:)
Maria Striki	(Advisor: Baras	Proposal: Fall 2003, Thesis:)
Ming-Yung Ko	(Advisor: Bhattacharyya	Proposal: Fall 2003, Thesis:)
Vida Kianzad	(Advisor: Bhattacharyya	Proposal: Fall 2003, Thesis:)
Shanhan Yang	(Advisor: Baras	Proposal: Spring 2003, Thesis:)
Zhu Han	(Advisor: Liu	Proposal: Fall 2001, Thesis: Fall 2003)
Neal Bambha	(Advisor: Bhattacharyya	Proposal: Fall 2001, Thesis: Fall 2003)
Himanhshu Khurana	(Advisor: Gligor	Proposal: Summer 2001, Thesis: Summer 2002)
Nitin Chandrachoodan	(Advisor: Bhattacharyya	Proposal: Thesis: Summer 2002)

M.S. (thesis defense of 10 students)

Fuat Keceli	(Advisor: Bhattacharyya	Summer 2004)
Fang Liu	(Advisor: Vishkin	Spring 2004)
Gautam Muralidharan	(Advisor: Gligor	Winter 2004)
Joseph Nuzman	(Advisor: Vishkin	Fall 2003)
Ohm Tuaycharoen	(Advisor: Jacob	Summer 2003)

Brinda Ganesh	(Advisor: Jacob	Fall 2002)
Paul Kohout	(Advisor: Jacob	Fall 2002)
Vinod K. Gupta	(Advisor: Barua	Fall 2002)
Deepak N. Agarwal	(Advisor: Yeung	Spring 2002)
Sumit Lohani	(Advisor: Bhattacharyya	Fall 2001)

M.S. Scholarly Paper (2nd reader of 4 students)

Vincent Chan	(Summer 2005)
Donald Lowe	(Spring 2004)
Shih-Ching Yu	(Fall 2002)
Michael J. Hilton	(Fall 2001)

4. Service

a. University

- Fall 2001 – Spring 2003: University Senate, Educational Affairs Committee
- Fall 2002 – present: Undergraduate Affair Committee (Dept. of ECE)
- Fall 2003 – Spring 2004: Graduate Studies and Research Committee (Dept. of ECE)
- March, 2002 – 2005: Electrical and Computer Engineering undergraduate telemarketing campaign
- Fall 2002 – Spring 2004: Contributed to building the database of foreign schools where graduate applicants finish their B.S./M.S. degrees (schools of P.R.China)

b. Professional

- **General Chair/Co-Chair**

GLSVLSI'06: 16th IEEE /ACM Great Lakes Symposium on VLSI 2006 (co-chair)

- **Technical Program Chair/Co-Chair**

GLSVLSI'05: 15th IEEE /ACM Great Lakes Symposium on VLSI 2005 (co-chair)

- **Technical Program Committee Member**

CASES'05: International Conference on Compilers, Architecture, and Systems for Embedded Systems

MSE'05: IEEE International Conference on Microelectronics Systems Education

GLSVLSI ('03, '04, '05): (13th, 14th, 15th) IEEE /ACM Great Lakes Symposium on VLSI (Local Arrangement Chair and Registration Chair in 2003, and Publication Chair in 2004)

ASAP ('03, '04, '05): (14th, 15th, 16th) IEEE International Conference on Application-specific Systems, Architectures and Processors

ISC'02: Information Security Conference

ISCAS ('02,'04,'05): (52nd, 54th, 55th) IEEE International Symposium on Circuits and Systems

- **Conference Session Chair**

GLSVLSI'05: 15th IEEE /ACM Great Lakes Symposium on VLSI, Chicago, IL, April 2005
GLSVLSI'04: 14th IEEE /ACM Great Lakes Symposium on VLSI, Boston, MA, April 2004
GLSVLSI'03: 13th IEEE /ACM Great Lakes Symposium on VLSI, Washington, DC, April 2003
ASAP'02: 13th IEEE International conference on Application-specific Systems, Architectures and Processors, San Jose, CA, July 2002
DAC'02: 39th ACM/IEEE Design Automation Conference, New Orleans, LA, June 2002
ISCAS'02: 52nd IEEE International Symposium on Circuits and Systems, Scottsdale, AZ, May 2002

- **Editorship**

Guest editor: special issue on “Embedded DSP Systems”, *EURASIP Journal on Embedded Systems*, 2005

- **Journal Reviewer**

ACM Transactions on Embedded Computing Systems
EURASIP Journal on Embedded Systems
IEEE Transactions on CAD of Integrated Circuits and Systems
IEEE Transactions on Computers
IEEE Transactions on Mobile Computing
IEEE Transactions on Multimedia
IEEE Transactions on VLSI Systems
IEEE Computer Magazine
IEEE Design and Test Magazine
International Journal of Embedded Systems
Journal of VLSI Signal Processing

- **Conference Reviewer**

ASAP: IEEE International Conference on Application-specific Systems, Architectures and Processors
CASES: International Conference on Compilers, Architecture, and Systems for Embedded Systems
DAC: ACM/IEEE Design Automation Conference
GLSVLSI: IEEE /ACM Great Lakes Symposium on VLSI
ICCAD: IEEE/ACM International Conference on Computer Aided Design
IHW: Information Hiding Workshop
ISC: Information Security Conference
ISCAS: IEEE International Symposium on Circuits and Systems
ISLPED: ACM/IEEE International Symposium on Low Power Electronics and Design
MSE: IEEE International Conference on Microelectronics Systems Education
SIGCSE: ACM SIGCSE Technical Symposium on Computer Science Education

- **Review Panel Member**

NASA Low Power Microelectronics Review Panel, Leesburg, VA, December 9–11, 2003