Big Memories

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OUTLINE
• The Capacity Problem
• Solution I: BOB Memory Systems
• Solution II: Hybrid Memory Cube
• Solution III: Non-volatile Main Memories
The Capacity Problem

Two DDR2-400 DIMMs

Four DDR2-400 DIMMs

The Capacity Problem

... but wait, there's more:
Attempts at a Solution

- Highly Engineered DIMMs (can cost $1000+ per DIMM)
- Fully-Buffered DIMM (pushes the power envelope)

JEDEC DDRx
~10W/DIMM, ~20W total

FB-DIMM
~10W/DIMM, ~300W total
Observations

- Cannot increase power significantly (e.g. to CPU scale)
- Cannot sacrifice aggregate bandwidth
- Need to approach commodity pricing
- Future-proof design would be highly desirable
Solution I: BOB

Buffer On (mother-)Board

IBM Power 795

Intel SMI/SMB

AMD G3MX
Solution I: BOB

Buffer On (mother-)Board
Solution I: BOB

Buffer On (mother-)Board

Impact of Request and Response Link Bus
8 Channels of DDR3-1600

Bandwidth/CPU Pin vs. Memory System Power

Pareto Frontier
Solution II: Micron HMC

Hybrid Memory Cube

- DRAM
- Slice
- TSVs
- Slice Controller
- Logic Layer & Crossbar Switch
- SerDes Buffers
- Response Link
- Request Link
- ...

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Solution II: Micron HMC
A single-chip BOB system
Solution II: Micron HMC

Hybrid Memory Cube

- DRAM Slice
- TSVs
- Slice Controller_0
- Slice Controller_1
- Slice Controller_2
- Slice Controller_n
- Logic Layer & Crossbar Switch
- SerDes Buffers
- Response Link
- Request Link

...
Solution II: Micron HMC

Bandwidth Scaling Comparison

HPCCG

STREAM

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<th>Bandwidth (GB/s)</th>
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Time (ms)

Time (ms)
Solution II: Micron HMC

![Graph showing Bandwidth and Latency over time for different configurations: BOB, BOB AMO, HMC, HMC AMO. The graph compares the performance of these configurations over a 25,000 ms time span.]

- Bandwidth (GB/s) values range from 1.1 to 1.7.
- Latency values range from 36 to 52 μs.
- The graph shows that BOB AMO and HMC AMO configurations consistently have lower latency compared to BOB and HMC configurations.

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SLIDE13
Obvious Conclusions II

• Flash/NV is inexpensive, is fast (rel. to disk), and has better capacity roadmap than DRAM
• Make it a first-class citizen in the memory hierarchy
• Access it via load/store interface, use DRAM to buffer writes, software management
• Probably reduces capacity pressure on DRAM system

Can have TB-scale DIMMs today
Solution III: Non-Volatiles

The design of SSDs involves several key components:

- **Core i7 CPU**: Central Processing Unit
- **Memory Controller**: Manages memory access
- **PCle Controller**: Controls PCIe operations
- **DDR3 Channel**: Connects to DRAM DIMMs
- **ONFI**: Standards for interface
- **SSD Controller**: Manages SSD operations
- **NAND Devices**: Storage medium
- **PCle Solid State Drive**: SSDs in PCIe interface
- **NV DIMM**: Non-Volatile Memory DIMM

The SSD controller also typically has a small amount of memory to perform tasks such as memory mapping, garbage collection, and access scheduling. These SSDs leverage multiple devices to achieve high throughputs, often with bandwidths of up to 200 MB/s. Furthermore, a new standard, ONFi 2.1 or Toggle Mode DDR, has been introduced to fully expose the improved performance of the flash devices.

As transfer times to such cards were less important than their capacity, until recently, NAND flash chips utilized a 40 MHz frequency. However, newer flash chips are capable of faster data transfers and improve overall performance when faster frequencies are used. The potential of the flash array will soon be utilized to provide faster access and lower latency.

This was also acceptable for some time as the access latency and the capacity of SSDs were large enough. However, as transfer times began to matter, the asynchronous interface was the primary bottleneck in SSDs. As a result, newer flash chips are capable of faster access, and older standards such as ONFi 2.1 or Toggle Mode DDR are increasingly being replaced with faster standards.
Solution III: Non-Volatiles

Performance normalized to that of TB-sized DRAM system
Bottom Line

- All three solutions are composable (this is GOOD)
- Power problem: solvable
- Bandwidth problem: solvable
- Cost problem: solvable
- HMC-style generic interface is future-proof by definition
Thank You!

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