Software-Managed Address Translation

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OUTLINE:

• Background & Motivation
• Softvm Design
• Experiments & Results

Historical Perspective

MIPS:
• HW page-table-walking unnecessary

SPUR:
• HW storage for PTEs unnecessary

VMP:
• Software-controlled caches work

CONCLUSION:
Can get rid of TLB altogether
SOFTVM Architecture

Match?
Protection Violation?

V-Tag
Pr

Cache Block (Data)

DIRECT-MAPPED CACHE

Match?

CPU

CACHE MISS

EXCEPTION

CACHE DATA

SOFTVM Miss

CPU

CACHE MISS

CACHE DATA

Virtual Address

Offset

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User Table

Root Table

BASE

PHYSICAL ADDR

Page Frame

PHYSICAL & VIRTUAL ADDR
Cost of Software Solution

Cost to handle TLB Miss: ~12 cycles
- Build PA & Load RPTE
- Build PA & Load UPTE
- Insert UPTE into TLB
- Retry Load

Cost to handle Cache Miss: ~15 cycles
- Build PA & Load RPTE
- Build PA & Load UPTE
- Prepare caches for USER-DATA
- Build PA & Load USER-DATA
- Retry Load

Cost vs. Cache Size

[Graph showing hit rate and cycles per cache miss against cache size, with lines indicating D-CACHE HIT RATE, I-CACHE HIT RATE, COST PER CACHE MISS, and COST PER INSTRUCTION.]
Experiments

Modified 32-BIT PowerPC Architecture, MIPS-like Page Table

Trace-Driven Simulations:
- L1 Cache (20): 2—256 KBytes
- L2 Cache (100): 1, 2, 4 MBytes
- Linesizes: 16—128 Bytes

RESULTS:
- Softvm: 0.1 to 5% Overhead
- Mach+MIPS: 5 to 10% Overhead
- Ultrix+MIPS: 2% Overhead

Results

L1 Caches: 16/16KB D/I, 32-byte linesize
L2 Caches: 64-byte linesize
Potential Problem: STREAM

MULTIMEDIA HAS NO TEMPORAL LOCALITY

WORST-CASE SCENARIO:
Take an exception for every cache line

SOLUTIONS:
• Prefetch buffers
• Prefetch into L2 cache
• Provided unmapped regions to user

Design Considerations

LARGE VIRTUAL CACHES:

Synonym Problem

SOLUTION:
Segmentation
or
Large ASIDs w/ Flat Address Space

DRAWBACK:
Increases size of cache tags
Conclusions

TLB Elimination is Possible

**Cycle Time** can **DECREASE**

**Performance** can **INCREASE**

Support for Multimedia Possible

Software-Managed: **FLEXIBILITY**