CS-590.26, Spring 2014

High Speed Memory Systems: Architecture and Performance Analysis

DRAM Device Circuits and Architecture

Credit where credit is due:
Slides contain original artwork (© Jacob, Wang 2005)
Overview
Storage Cells

3T1C storage cell (original DRAM)

1T1C storage cell (classic DRAM)

6T storage cell (classic SRAM)

DRAM: Dynamic Random Access Memory

How long does “memory storage” last?

Cell capacitance vs Leakage current
Storage Cell Structure I

plate capacitor

\[ C = \varepsilon \frac{A}{d} \]

Shrinking DRAM devices means reduced cross section (area)

- above silicon in poly
- below silicon surface in trench
Storage Cell Structure II

[Diagram of storage cell structure with labeled parts such as bitline, wordline, access transistor, stacked capacitor, poly 1, poly 2, poly 3, metal 1 bitline, etc.]

[Further detail of the structure with labels for deep trench, buried n⁺ plate, insulating dielectric, poly-silicon storage, and much deeper trench.]
DRAM Array I

8F^2 cell
(F = feature size. 90nm etc)

Polycide Bitlines

Unlayered DRAM Cell Array
DRAM Array II

Note the direction of the arrows—storage via capacitance
DRAM Array III (folded bitline)

2 Bitline lanes through each cell (larger cell size)
Cell size: typically 8 $F^2$
Better noise tolerance (common mode rejection)
DRAM Array IV (Open Bitline)

- Dummy structures at array edges
- 1 Bitline lane through each cell
  Cell size: typically 6 \( F^2 \)
- Bitline pairs come from different array segments

Challenge: How to get good noise tolerance AND small cell size?
Sense Amplifier

Differential

Control Signals
**Array Precharge**

**Precharge**

Assert equalize, Array precharged to \( V_{\text{ref}} \) (typically \( V_{\text{cc}}/2 \))

\[
0 \quad V_{\text{ref}^-} \quad V_{\text{ref}} \quad V_{\text{ref}^+} \quad 1
\]

Voltage color chart
Row Access 0

about to select this row (wordline)

timeline
An Aside: the Sense Amp

Bitline

SAN

goes to GND

Bitline

SAP

goes to Vcc
An Aside: the Sense Amp

Bitline

SAN

goes to GND

SAP

goes to Vcc
Row Access 0

about to select this row (wordline)

timeline
Row Access I

selected row (wordline) activated

timeline

\begin{align*}
&v_{cc} + v_t \\
&v_{cc} \\
&(v_{ref}) \frac{v_{cc}}{2} \\
&v_{cc}/2 \\
&Gnd
\end{align*}

Access \quad Sense \quad Restore \quad Precharge

\begin{align*}
t_{RCD} &\quad t_{RAS} &\quad t_{RP}
\end{align*}
Row Access II (sense)

SAN and SAP control signals active lower NFet more conductive, upper PFet more conductive. Bitline pairs slammed to opposite voltage rails, then upper NFet and lower PFet shut off completely.

Timeline

0 $V_{\text{ref}^-}$ $V_{\text{ref}}$ $V_{\text{ref}^+}$ 1

Voltage color chart

$V_{cc} + V_t$

$V_{cc}$

$(V_{\text{ref}}) V_{cc}/2$

Gnd

Access $t_{RCD}$

Sense

Restore

Precharge $t_{RP}$
Row Access III (Restore)

Wordline kept open, now bitline potential drives the full voltage level “1” back into cell. If the column is selected, data is driven out to rest of the world.

Voltage color chart
Write (over old data)

Wordline is still open, input write driver drives the full voltage level “0” into cell.

Voltage color chart

0  \( V_{\text{ref}}^- \)  \( V_{\text{ref}} \)  \( V_{\text{ref}}^+ \)  1

Timeline

Access  Sense  Restore  Write Recovery  Precharge

\( t_{\text{WR}} \)  \( t_{\text{RP}} \)
Decoders and Redundancy

Challenge: How to get good yield and tolerate *some* defect?
Programmable Decoders I

standard decoder (each row has one)

spare decoder (each spare row has one)

(laser) programmable link

functionally equivalent to NOR gate with output that can be disabled by laser (or fuse)

functionally equivalent to NOR gate with inputs that can be selectively disabled
Programmable Decoders II

4 address bits select 1 of 16 rows.

Suppose that row 0b0100 is defective.

- Blast it with laser
- Replace standard decoder with spare row decoder

\[ a_3 + a_2 + a_1 + a_0 \]
Device Control Logic

SDRAM

Control Logic

FPM

Remember SAN and SAP? Something has to control sequence and timing
Mode Register

Modern DRAM devices (SDRAM, Direct RDRAM, DDRx SDRAM, etc. have programmable behaviour)
Load value from address bus with special command.
Data I/O

2N Bit prefetch in DDR SDRAM devices
4N in DDR2 SDRAM devices, and
8N in DDR3 SDRAM devices
Allows “core” to run at slower datarates while interface datarate cranks up.
drawback - minimum burst lengths
(loss of “randomness”)
SDRAM Device

Find bank 0, row 0x02F1, column 0x0EA and get an A
SDRAM Evolution

Micron DDR1

Hynix DDR2

Micron DDR3

GDDR5
## Package and Pincount I

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<th>2014</th>
<th>2017</th>
<th>2020</th>
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<tr>
<td>Memory device pin cost (cents/pin)</td>
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<td>0.20 - 0.30</td>
<td>0.20 - 0.26</td>
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2012 ITRS Roadmap

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**Package Evolution**
(higher pin count, higher datarate)
(higher costs, testing etc.)
Package and Pincount II

SDRAM “Same pinout”, except for data bus