

CURRICULUM VITAE
Rajeev Barua

Certification. I have read the following and certify that this curriculum vitae is a current and accurate statement of my professional record.

Signature _____ Date _____

1. Personal Information

a. Education

- August 1992 **B.Tech.** Indian Institute of Technology, New Delhi.
Department of Computer Science and Engineering
(Awarded President of India's Gold Medal for being ranked first in University with GPA=9.86/10)
- May 1994 **M.S.** Massachusetts Institute of Technology
Department of Computer Science and Electrical Engineering
Advisor: Prof. Anant Agarwal
Dissertation: "Global partitioning of Parallel Loops and Data Arrays for Caches and Distributed Memory in Multiprocessors"
GPA at MIT (MS + PhD): 4.97/5.0
- Jan 2000 **Ph.D.** Massachusetts Institute of Technology
Department of Computer Science and Electrical Engineering
Advisors: Prof. Saman Amarasinghe and Prof. Anant Agarwal
Major field: Compilers and Computer Architecture.
Minor fields: Finance and Accounting
Dissertation: "Maps: A Compiler-Managed Memory System for Software-Exposed Architectures"
GPA at MIT (MS + PhD): 4.97/5.0

b. Experience

- 7/2006 – present *Associate Professor,*
Department of Electrical and Computer Engineering,
University of Maryland, College Park
- 1/2000 – 6/2006 *Assistant Professor,*
Department of Electrical and Computer Engineering,
University of Maryland, College Park
- 5/2000 – present *Affiliate Professor,*

**Department of Computer Science,
University of Maryland, College Park**

- 8/1992 – 1/2000 *Research Assistant, Laboratory for Computer Science,
Massachusetts Institute of Technology*
- 1/1995 – 5/1995 *Teaching Assistant, Laboratory for Computer Science,
Massachusetts Institute of Technology*
- Summer, 1993 *Intern, Motorola Cambridge Research Center, Cambridge, MA*
- Summer, 1991 *Intern, Central Railway Information Systems, New Delhi, India*
- Summer, 1990 *Intern, Indian Institute of Technology CAD Laboratory, New Delhi, India*

2. Research, Scholarly, and Creative Activities

- *My name and the name of my students at the University of Maryland are in boldface.*
- *Up-to-date list & full text of publications available at <http://www.ece.umd.edu/~barua>.*

a. Refereed Journal Articles

- A.1 E. Waingold, M. Taylor, V. Sarkar, W. Lee, V. Lee, J. Kim, M. Frank, P. Finch, D. Srikrishna, **R. Barua**, J. Babb, S. Amarasinghe, and A. Agarwal. “Baring it all to Software: The Raw Machine.” *IEEE Computer*, September 1997, pp. 86-93.
- A.2 **R. Barua**, W. Lee, S. Amarasinghe and A. Agarwal. “Compiler Support for Scalable and Efficient Memory Systems.” *IEEE Transactions on Computers* Special Issue on Memory Systems, 50(11), pp 1234-1247, November 2001.
- A.3 **O. Avissar**, **R. Barua** and D. Stewart. “An Optimal Memory Allocation Scheme for Scratch-Pad Based Embedded Systems.” *ACM Transactions on Embedded Computing Systems (TECS)*, 1(1), pp. 6-26, November 2002.
- A.4 **Yi Zhang**, **Steve Haga**, and **Rajeev Barua**. “Execution History Guided Instruction Prefetching.” *Journal of Supercomputing*, 27(2), pp 129-147, February 2004. Kluwer Academic Publishers.

- A.5 **Steve Haga, Natasha Reeves, Rajeev Barua** and Diana Marculescu. “Dynamic Functional Unit Assignment for Low Power,” *Journal of Supercomputing*, 31(1), pp 47-62, January 2005, Kluwer Academic Publishers.
- A.6 **Steve Haga, Yi Zhang, Andrew Webber and Rajeev Barua.** “Reducing Code Size in VLIW Instruction Scheduling.” In *Journal of Embedded Computing*, 1(3), 2005, IOS Press, Amsterdam, The Netherlands.
- A.7 **Angel Dominguez, Sumesh Udayakumaran and Rajeev Barua.** “Heap Data Allocation to Scratch-Pad Memory in Embedded Systems.” In *Journal of Embedded Computing*, 1(4), pp 521-540, 2005, IOS Press, Amsterdam, The Netherlands.
- A.8 **Surupa Biswas, Thomas Carley, Matthew Simpson and Rajeev Barua.** “Memory Overflow Protection for Embedded Systems using Run-time Checks, Reuse and Compression.” In the *ACM Transactions on Embedded Computing Systems (TECS)*, 5(4), pp 719-752, November 2006.
- A.9 **Sumesh Udayakumaran, Angel Dominguez and Rajeev Barua.** “Dynamic Allocation for Scratch-Pad Memory using Compile-Time Decisions.” In *ACM Transactions on Embedded Computing Systems (TECS)*, 5(2), pp 472-511, May 2006.
- A.10 **Bhuvan Middha, Matthew Simpson and Rajeev Barua .** “MTSS: Multi Task Stack Sharing for Embedded Systems.” In *ACM Transactions on Embedded Computing Systems (TECS)*, 7(4), Article 46, pp 1-37, July 2008.
- A.11 **Nghi Nguyen, Angel Dominguez, and Rajeev Barua.** “Memory Allocation for Embedded Systems with a Compile-Time-Unknown Scratch-Pad Size.” In *ACM Transactions on Embedded Computing Systems (TECS)*, 8(3), pp 1-32, April 2009.

b. Journal Articles in review

c. Articles in Refereed Symposia, Conferences and Workshops

In the Computer Systems field, publications in the top journals take between 2 and 4 years from submission to publication. Given the fast pace of the field, high quality conferences have become nearly as important, and in some cases more important, than journals in disseminating new ideas in Computer Systems. To ensure the quality of articles appearing in highly competitive conferences, full manuscripts (6000-9000 word papers, not extended abstracts) must be submitted. Each paper usually receives three to six full-length reviews. Furthermore, the acceptance rates are low, around

20-30% for the most competitive conferences. Highly competitive conferences listed below include ISCA, ASPLOS, HPCA, ICS, CASES, RTSS and DATE – each one is a leading top-tier conference in its field. The acceptance rate for a conference is listed below if it was published in its proceedings, regardless of whether it was low or high.

- C.1 **R. Barua**, D. Kranz and A. Agarwal. “Communication-Minimal Partitioning of Parallel Loops and Data Arrays for Cache-Coherent Distributed-Memory Multiprocessors.” *Proceedings of Languages and Compilers for Parallel Computing (LCPC)*, pp 350-368, Springer Verlag, Berlin, Germany, August 1996. (19 pages).

(Acceptance rate not listed in proceedings)

- C.2 J. Babb, M. Frank, E. Waingold, **R. Barua**, M. Taylor, J. Kim, D. Srikrishna, P. Finch, and A. Agarwal. “The RAW Benchmark Suite: Computation Structures for General Purpose Computing.” *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp 134-143 Napa Valley, CA, April 1997. (10 pages)

(25 papers accepted out of 56 papers submitted – 45 % acceptance rate)

- C.3 A. Agarwal, S. Amarasinghe, **R. Barua**, M. Frank, W. Lee, V. Sarkar, D. Srikrishna and M. Taylor. “The Raw Compiler Project.” *Proceedings of the Second SUIF Compiler Workshop*, Stanford, CA, August 21-23, 1997. (12 pages)

(Acceptance rate not listed in proceedings)

- C.4 F. T. Chong, **R. Barua**, F. Dahlgren, J. Kubiawitz, and A. Agarwal. “The Sensitivity of Communication Mechanisms to Bandwidth and Latency.” *Proceedings of 4th Int’l Symposium on High Performance Computer Architecture(HPCA)*, pp 37-46, Las Vegas, NV, Feb 1-4, 1998. (10 pages)

(31 papers accepted out of 141 papers submitted – 22 % acceptance rate)

- C.5 W. Lee, **R. Barua**, D. Srikrishna, J. Babb, V. Sarkar, and S. Amarasinghe. “Space-Time Scheduling of Instruction-Level Parallelism on a Raw Machine.” *Proceedings of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, pp 46-57, San Jose, CA, October, 1998. (12 pages)

(28 papers accepted out of 123 papers submitted – 22 % acceptance rate)

- C.6 **R. Barua**, W. Lee, S. Amarasinghe and A. Agarwal. “Memory Bank Disambiguation using Modulo Unrolling for Raw Machines.” *Proceedings of the ACM/IEEE Fifth International Conference on High-Performance Computing (HiPC)*, pp 212-220, December, 1998. (9 pages)
(62 papers accepted out of 104 papers submitted – 59 % acceptance rate)
- C.7 J. Babb, M. Rinard, A. Moritz, W. Lee, M. Frank, **R. Barua**, and S. Amarasinghe. “Parallelizing Applications Into Silicon.” *Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, pp 70-80, Napa Valley, April 1999. (11 pages)
(Acceptance rate not listed in proceedings)
- C.8 **R. Barua**, W. Lee, S. Amarasinghe and A. Agarwal. “Maps: A Compiler-Managed Memory System for Raw Machines.” *Proceedings of the Twenty-Sixth International Symposium on Computer Architecture (ISCA)*, pp 4-15, Atlanta, GA, May, 1999. (12 pages)
(26 papers accepted out of 135 papers submitted – 19 % acceptance rate)
- C.9 **O. Avissar**, **R. Barua** and D. Stewart. “Heterogeneous Memory Management of Embedded Systems.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems(CASES)*, pp. 34-43, Atlanta, GA, November, 2001. (10 pages)
(28 papers accepted out of 80 papers submitted – 35 % acceptance rate)
- C.10 **Steve Haga and Rajeev Barua**. “EPIC Instruction Scheduling Based on Optimal Approaches.” *1st Annual Workshop on Explicitly Parallel Instruction Computing Architectures and Compiler Technology (EPIC)*, Austin, TX, December, 2001. (10 pages)
(8 papers accepted out of 23 papers submitted – 35 % acceptance rate)
- C.11 **T.V.K Gupta, Roberto Ko and Rajeev Barua**. “Compiler-directed Customization of ASIP Cores.” *Proceedings of Tenth ACM/IEEE Int’l Symposium on Hardware/Software Codesign (CODES)*, pp. 97-102, Estes Park, CO, May, 2002. (6 pages)
(25 papers accepted out of 76 papers submitted – 33 % acceptance rate)
- C.12 **Zhang Yi, Steve Haga and Rajeev Barua**. “Execution History Guided Instruction Prefetching.” *Proceedings of the Sixteenth ACM Int’l Conference on Supercomputing*, pp 199-208, New York City, NY, June 22-26, 2002. (10 pages)
(31 papers accepted out of 144 papers submitted – 22 % acceptance rate)
- C.13 **S. Haga, N. Reeves and R. Barua**. “Dynamic Functional Unit Assignment for Low Power.” *Proceedings of International Conference on Design, Automation and Test in*

Europe (DATE), pp 11052-11057, Munich, Germany, March 3-7, 2003. (6 pages)

(98 papers accepted out of 590 papers submitted – 17 % acceptance rate)

- C.14 **Sumesh Udayakumaran and Rajeev Barua.** “Compiler-Decided Dynamic Memory Allocation for Scratch-Pad Based Embedded Systems.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp 276-286, San Jose, CA, October 30-November 1, 2003. (11 pages)

(31 papers accepted out of 162 papers submitted – 19 % acceptance rate)

- C.15 **Tom Carley, Musa Ba, Rajeev Barua and Dave Stewart.** “Contention-Free Periodic Task Scheduler Medium Access Control in Wireless Sensor / Actuator Networks.” *Proceedings of The 24th IEEE Real-Time Systems Symposium (RTSS)*, pp 298-307, Cancun, Mexico, December 3-5, 2003. (10 pages)

(32 papers accepted out of 145 papers submitted – 22 % acceptance rate)

- C.16 **Surupa Biswas, Matthew Simpson, and Rajeev Barua.** “Memory Overflow Protection for Embedded Systems using Run-time Checks, Reuse and Compression.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp 280-291, Washington, DC, September 22-25, 2004. (12 pages)

(31 papers accepted out of 102 papers submitted – 30 % acceptance rate)

- C.17 **Bhuvan Middha, Matthew Simpson and Rajeev Barua.** “MTSS: Multi Task Stack Sharing for Embedded Systems.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, San Francisco, CA, September 25-27, 2005. (12 pages)

(31 papers accepted out of 101 papers submitted – 31 % acceptance rate)

- C.18 **Nghi Nguyen, Angel Dominguez and Rajeev Barua.** “Memory Allocation for Embedded Systems with a Compile-Time-Unknown Scratch-Pad Size.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, San Francisco, CA, September 25-27, 2005. (12 pages)

(31 papers accepted out of 101 papers submitted – 31 % acceptance rate)

- C.19 **Matthew Simpson, Bhuvan Middha and Rajeev Barua.** “Segment Protection for Embedded Systems Using Run-time Checks” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, San Francisco, CA, September 25-27, 2005. (12 pages)

(31 papers accepted out of 101 papers submitted – 31 % acceptance rate)

- C.20 **Sumesh Udayakumaran and Rajeev Barua.** “An Integrated Scratch-Pad Allocator for Affine and Non-affine Codes.” *Proceedings of International Conference on Design, Automation and Test in Europe (DATE)*, Munich, Germany, March 6-10, 2006. (6 pages)

(278 papers accepted out of 817 papers submitted – 34 % acceptance rate)

- C.21 **Nghi Nguyen, Angel Dominguez and Rajeev Barua.** “Scratch-Pad Memory Allocation without Compiler Supports for Interpreted-Language based Applications” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, Salzburg, Austria, October 1-3, 2007. (10 pages)

(22 full papers accepted out of 77 papers submitted – 28% acceptance rate)

- C.22 **Angel Dominguez, Nghi Nguyen and Rajeev Barua.** “Recursive Function Allocation to Scratch-Pad Memory for Embedded Systems” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, Salzburg, Austria, October 1-3, 2007. (10 pages)

(22 full papers accepted out of 77 papers submitted – 28% acceptance rate)

- C.23 **Kapil Anand and Rajeev Barua.** “Instruction Cache Locking inside a Binary Rewriter.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, Grenoble, France, October 11-16, 2009. (10 pages)

(24 full papers accepted out of 72 papers submitted – 33% acceptance rate)

d. Chapters in Books (Non-refereed)

- D.1 A. Agarwal, D. Kranz, **R. Barua** and Venkat Natarajan. “Optimal Tiling for Minimizing Communication in Distributed Shared-Memory Multiprocessors” Chapter 9, *Compiler Optimizations for Scalable Parallel Systems– Languages, Compilation Techniques and Runtime Systems*, LNCS Series 1808, Springer-Verlag, Berlin, Germany, 2001.

- D.2 **S. Haga, N. Reeves and R. Barua.** “Dynamic Functional Unit Assignment for Low Power.” In *Embedded Software for SoCs*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2003.

e. Non-refereed Research Publications

- E.1 **R. Barua** and V. Natarajan. “Loop and Data Partitioning in Distributed Memory Non-Cached Machines”. *Technical Report*, Motorola Cambridge Research Center, Cambridge, MA, Motorola Inc., August 1993. MCRC-TR-34.

- E.2 **R. Barua.** “Global Partitioning of Parallel Loops and Data for Caches and Distributed Memory in Multiprocessors.” *Masters Thesis*, MIT Laboratory for Computer Science, May 1994. MIT-LCS-TR-630.

- E.3 **R. Barua**, D. Kranz and A. Agarwal. “Addressing Partitioned Arrays in Distributed

Memory Multiprocessors - the Software Virtual Memory Approach.” *Proceedings of the MIT Student Workshop*, Wellesley, MA, Aug 1995.

- E.4 **R. Barua.** “Maps: A Compiler-Managed Memory System for Software-Exposed Architectures.” *Ph.D thesis*, MIT Laboratory for Computer Science, Jan 2000. MIT-LCS-TR-799.

f. Presentations

i. Invited talks

- F.1 “Maps : A Compiler-Managed Memory System for Raw Machines.” *College of Computing*, Georgia Institute of Technology, Atlanta, GA, March 18, 1999.
- F.2 “Maps : A Compiler-Managed Memory System for Raw Machines.” *System Research Laboratory*, Compaq Corporation, Palo Alto, CA, May 6, 1999.
- F.3 “Maps : A Compiler-Managed Memory System for Raw Machines.” *Cambridge Research Laboratory*, Compaq Corporation, Cambridge, MA, May 18, 1999.
- F.4 “Compiler Optimizations for Software-exposed Microprocessors.” *Product and Research Groups*, Intel Corporation, Santa Clara, CA, Sept 26, 2000.
- F.5 “EPIC Instruction Scheduling Based on Optimal Approaches.” *To Intel Research Groups worldwide*, Teleconference talk, February 25, 2002.
- F.6 “Memory Management for Embedded Systems.” *NASA Goddard and University of Maryland Technical Summit*, University of Maryland, College Park, April 23, 2002.
- F.7 “An Overview of Embedded Systems.” External speaker in class ENES 181, *Dialogue with the Dean*, University of Maryland, College Park, October 16, 2002.
- F.8 “Memory Allocation for Scratch-Pad Based Embedded Systems.” Invited Speaker, *Computer Architecture Seminar Series*. Division of Engineering and Applied Science, Harvard University, May 17, 2004.
- F.9 “Compiler technologies for efficiency and reliability in Embedded Systems.” Invited Speaker, *Computer Science and Artificial Intelligence Laboratory (CSAIL) seminar*, Massachusetts Institute of Technology, November 29, 2004.
- F.10 “Compiler technologies for efficiency and reliability in Embedded Systems.” Invited Speaker, *Computer Science department colloquium*, Rice University, March 9, 2005.
- F.11 “Beating the Desktop Legacy in Embedded Systems Design.” Invited Speaker, *ECE department seminar series*, University of Illinois, Urbana-Champaign, August 30, 2005.

ii. Conference and Workshop Presentations

- F.8 “Addressing Partitioned Arrays in Distributed Memory Multiprocessors - the Software Virtual Memory Approach.” *The Fifth Annual MIT Student Workshop*, Wellesley, MA, Aug 8, 1995.
- F.9 “Communication-Minimal Partitioning of Parallel Loops and Data Arrays for Cache-Coherent Distributed-Memory Multiprocessors.” *Ninth International Workshop on Languages and Compilers for Parallel Computing*, Santa Clara, CA, August 9, 1996.

- F.10 “Compiler-Managed Memory System on a Raw Machine.” *The Seventh Workshop on Scalable Shared-Memory Multiprocessors*, Barcelona, Spain, June 27, 1998.
- F.11 “Memory Bank Disambiguation using Modulo Unrolling for Raw Machines.” *The ACM/IEEE Fifth International Conference on High-Performance Computing (HiPC)*, Chennai, India, December 19, 1998.
- F.12 “Maps: A Compiler-Managed Memory System for Raw Machines.” *The Twenty-Sixth International Symposium on Computer Architecture*, Atlanta, GA, May 2, 1999.
- F.13* “Heterogeneous Memory Management of Embedded Systems.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 34-43, Atlanta, GA, November, 2001.
- F.14* “EPIC Instruction Scheduling Based on Optimal Approaches.” *1st Annual Workshop on Explicitly Parallel Instruction Computing Architectures and Compiler Technology (EPIC)*, Austin, TX, December, 2001.
- F.15* “Compiler-directed Customization of ASIP Cores.” *Proceedings of ACM/IEEE Int’l Symposium on Hardware/Software Codesig*, pp. 97-102, Estes Park, CO, May, 2002.
- F.16* “Execution History Guided Instruction Prefetching.” *Proceedings of the Sixteenth ACM Int’l Conference on Supercomputing*, New York City, NY, June 22-26, 2002.
- F.17* “Dynamic Functional Unit Assignment for Low Power.” *Proceedings of International Conference on Design, Automation and Test in Europe (DATE)*, Munich, Germany, March 3-7, 2003.
- F.18* “Compiler-Decided Dynamic Memory Allocation for Scratch-Pad Based Embedded Systems.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, San Jose, CA, October 30-November 1, 2003.
- F.19* “Contention-Free Periodic Task Scheduler Medium Access Control in Wireless Sensor / Actuator Networks.” *Proceedings of The 24th IEEE Real-Time Systems Symposium (RTSS)*, Cancun, Mexico, December 3-5, 2003.
- F.20* “Memory Overflow Protection for Embedded Systems using Run-time Checks, Reuse and Compression.” *Proceedings of the ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, Washington, DC, September 22-25, 2004.

*These conference talks were given by the student lead author listed in Section c. for the corresponding conference paper. However, in all cases, I was closely involved in creating the slides, and preparing the student through numerous practice talks.

g. Contracts and Grants

- National Science Foundation. Computer Systems Research Program. “*CSR: Small: Binary rewriting without relocation information.*” \$349,059. Principal Investigator.. (Sept 2009 – August 2012).

- DARPA AACE program. “AESOP: Adaptive Environment for Supercompiling with Optimized Parallelism.” UMD Principal Investigator. (UMD co-PIs: Rance Cleaveland (CS/ISR), Alan Sussman (CS/UMIACS)). UMD portion \$2.53 Million. (My portion \$1.34 Million) (2009-2013)
- National Science Foundation. Computer Systems Research Program. “CSR-PSCE,SM: Compiler-Directed System Optimization of a Highly-Parallel Fine-Grained Chip Multiprocessor.” \$400,000. Principal Investigator. (co-PI: Vishkin). (Sept 2008 – August 2011).
- National Science Foundation. Embedded and Hybrid Systems Program. “Memory management as a run-time service”. \$180,000, Principal Investigator. (August 2007 – July 2010).
- U.S. Department of Defense. “Technology study of a general-purpose extremely fine-grained multithreaded computing system.” \$745,877. Senior Personnel. PI: Vishkin (September 2005 – March 2007).
- National Science Foundation. Major Research Instrumentation Program. “Development of Energy-Efficient Embedded Systems for Wireless Sensor Networks”. \$400,000. Co-Principal Investigator. (PI: Ephremides. Other Co-PIs and senior personnel: Abshire, Jacob, Petrov, Qu, Ulukus and Vishkin). (August 2005 – July 2009).
- National Science Foundation. Embedded and Hybrid Systems Program. “Dynamic Memory Management for Embedded Systems”. \$100,000, Principal Investigator. (August 2004 – July 2006).
- Maryland Technology Development Corporation. “A Dynamic Memory Allocator for Embedded Systems with Scratch-Pad Memory.” \$50,000, Principal Investigator. (September 2004 – September 2005).
- National Science Foundation. Information Technology Research Program. “ITR: PRAM On-Chip”. \$750,000, Co-Principal Investigator. (PI: Vishkin. Other Co-PIs: Qu, Jacob and Franklin). (September 2003 – August 2007).
- National Science Foundation. Embedded and Hybrid Systems Program. “CAREER: Synthesis-assistance and Compilation Software for Embedded Systems”. \$300,000, Principal Investigator. (February 2002 – January 2007).
- University Of Maryland Minta Martin Research Award, “Compilation for Embedded Systems”. \$40,000. Principal Investigator. (June 2000 – June 2001).

h. Fellowships, Prizes, and Awards.

- Finalist, 2004 Inventor of the Year Award

This is an annual award given by the Office of Technology Commercialization at the University of Maryland. We were one of three finalists among 35 inventions filed with OTC in 2004 in the Information Science category. Our invention, IS-2004-043, is titled “A Dynamic Memory Allocator for Embedded Systems with Scratch-Pad Memory.”

- George Corcoran Memorial Award, September 2003.

“Presented to Professor Rajeev Barua for significant contributions to Electrical and Computer Engineering Education, in recognition of teaching and education leadership at the College Park campus, effective contributions at the national level, and creative and other scholarly activities related to Electrical and Computer Engineering education.”

- National Science Foundation Career Award, February 2002.

“The Faculty Early Career Development (CAREER) Program ... offers the National Science Foundation's most prestigious awards for new faculty members. The CAREER program recognizes and supports the early career-development activities of those teacher-scholars who are most likely to become the academic leaders of the 21st century.”

- One of the my undergraduate research interns, Kaushik Veeraraghavan, received the “Best Project” award in the College-sponsored ASPIRE program for 2002. (Also mentioned in Undergraduate projects).
- President of India Gold Medal, 1992 (*For 1/300 rank, B.Tech class of '92 at the Indian Institute of Technology (IIT), Delhi.*)
- National Champion, Rotary Club debating competition, 1988, New Delhi, India.

i. Patents

- Rajeev Barua and Sumesh Udayakumaran. “Compiler-driven dynamic memory allocation methodology for scratch-pad based embedded systems.” United States Patent #7,367,024, April 29, 2008.

3. Teaching and Advising

a. Courses taught

Semester	Course number	Course title	Credit hours	Enroll-ment	Evaluation (max:4.0)
Spring 00	ENEE759C	Compiler Optimizations for Modern Architectures	3	14	3.68
Fall 00	ENEE646	Digital Computer Design	3	69	2.99
Fall 00	ENEE698B	Computer Engineering Seminar	1	17	N/A
Spring 01	ENEE244	Digital Logic Design	3	65	3.20
Fall 01	ENEE350H	Computer Organization	3	13	3.76
Spring 02	ENEE244	Digital Logic Design	3	75	3.38
Fall 02	ENEE350H	Computer Organization	3	28	3.33
Spring 03	ENEE759C	Compiler Optimizations for Modern Architectures and Embedded Systems	3	9	3.79
Fall 03	ENEE350H	Computer Organization	3	35	3.08
Spring 04	ENEE 446	Digital Computer Design	3	40	3.23
Fall 04	ENEE 350H	Computer Organization	3	23	3.66 *
Spring 05	ENEE 759C	Compiler Optimizations for Modern Architectures and Embedded Systems	3	8	3.36
Fall 05	ENEE 350H	Computer Organization	3	5	3.33
Spring 06	ENEE 244	Digital Logic Design	3	46	3.52 †
Fall 06	ENEE 350H	Computer Organization	3	15	3.52 §
Spring 07	ENEE 759C	Compiler Optimizations for Modern Architectures and Embedded Systems	3	20	3.31
Fall 07	ENEE 350H	Computer Organization	3	30	3.23
Spring 08	ENEE 446	Digital Computer Design	3	32	3.57
Fall 08	ENEE 459R	Compilers	3	13	3.42
Spring 09	ENEE 446	Digital Computer Design	3	27	3.37

* Highest teaching evaluation score in the department in a 300-level course among twenty such courses taught in that semester.

† Second-highest teaching evaluation score in the department in a 200-level course among seven such courses taught in that semester.

§ Third-highest teaching evaluation score in the department in a 300-level course among twenty such courses taught in that semester.

Types of courses

Undergraduate core classes: ENEE244, ENEE 446

Undergraduate core for honors students: ENEE350H

Graduate core classes: ENEE646

Graduate special-topics and seminar classes: ENEE759C, ENEE698B

b. Course or Curriculum Development.

New courses offered:

- In Spring 2000, I designed and taught a new course ENEE759C, “Compiler Optimizations for Modern Architectures”. This is the first course in the university that describes how compiler techniques apply to particular computer architectures, filling a significant gap in the course options available to our graduate students.
- In Fall 2008, I designed and taught a new course, ENEE 459R, “Compilers”. This is the first undergraduate compiler course in our department. It was created in response to a unanimous vote by the computer engineering faculty that such a course should be designed and made a future core class in the undergraduate curriculum for CE students. Besides lectures, it included four homeworks, a significant software project, a midterm, and a final exam.

Significant revisions of existing courses:

- In Spring 2003, I significantly revised the curriculum of the course ENEE759C, and renamed it to “Compiler Optimizations for Modern Architectures and Embedded Systems”. About 50% of the course curriculum was completely new, emphasizing exciting new developments in Embedded Systems. To accommodate this material, some older technologies for desktop systems were deleted.
- In Fall 2004, all the homeworks and the project in ENEE 350H were re-designed with a significantly different approach, format and difficulty level. The students apparently liked it, since the teaching evaluation increased to 3.66 from 3.08 the last time I taught the course.
- In Spring 2006, all the homeworks in ENEE 244 were also re-designed with a significantly different approach, format and difficulty level. Consequently, the teaching evaluation increased to 3.52 from 3.38 the last time I taught the course.
- In Spring 2007, the reading list for ENEE 759C was completely revised with most of the papers being new. The lecture content was increased, and the number of homeworks significantly increased. The number of written reports on papers was cut.

Department-wide:

- Served on a committee in 2003 mandated to examine and recommend changes to the undergraduate curriculum in Electrical Engineering/Computer Engineering at the University of Maryland. (Also mentioned in service).

c. Manuals, Notes, Software, Webpages, and Other Contributions to Teaching.

Software

- I installed the SUIF compiler software on glue system for use in ENEE759C (Spring 2000). Students completed a end-of-term project using the software. The software has since also been used by Prof. Yeung in his research.
- I installed the DLX software (compiler + simulator) for the first time on the glue system for use in ENEE350H (Fall 2001). Since a release for the Solaris Operating System was not available, the installation involved a substantial porting and debugging effort. Students completed one short and one substantial assignment using the software.

Manuals

- I wrote extensive tutorial-style documentation for the SUIF software that I installed on glue, for a total of about ten pages. Students in ENEE759C as well as other users in the university have reported that they found the documentation very useful.

Webpages

- All my courses have class websites containing most course material online, including course information, schedules, syllabi, homeworks, solutions to homeworks and exams, and class announcements. When applicable, the following are also provided online: reading lists, on-line links to papers in reading list, project information and instructions on using course software.

Design of end-of-term class projects

- I designed a substantial month-long end-of-term project for ENEE759C that involved writing a new compiler pass using the SUIF compiler software. I wrote documentation and test examples for the project. The students chose a project among three offered, and worked in groups to complete the work. The project exposed the students to the structure of a modern compiler, and taught them how to extend its functionality by implementing compiler transformations
- I designed a three-week long project for ENEE350H that involved writing a simulator for virtual memory. I wrote four pages of documentation describing exactly what aspects of virtual memory to model, and the general approach to writing such a simulator. I described a set of experiments to perform using the simulator.
- I designed a month-long end-of-term compiler software project for ENEE 459R. It used the SUIF software that I had earlier installed on glue.

d. Teaching Awards and Other Special Recognition.

- George Corcoran Memorial Award, September 2003. (Note, this award also listed in Section 2.h). This is an award given annually to an Assistant Professor in the ECE department for excellence in teaching.

- NSF Career Award, 2002. Although this is primarily a research award, it has a significant teaching component. One of the reviewers (#2 on Fastlane) said “the proposal includes a strong educational component, with application to graduate, undergraduate, and high-school students.”

e. Advising: Other Than Research Direction.

Undergraduate

- I have acted as a faculty mentor for over 30 undergraduate students in the ECE department in the last three years.

Graduate

- I have acted as academic advisor for over 20 graduate students in the ECE department in the last five years.

f. Advising: Research Direction.

Undergraduate students

(Sum = Summer, Spr = Spring)

<i>Student</i>	<i>Duration</i>	<i>Topic of Research Project</i>
Adam Archer	Summer 00	“Porting SUIF to the IA-64 Architecture”
Wesley Maness	Summer 00	“Porting SUIF to the MIPS Architecture”
Roberto Ko ^s	Summer 01	“Building a DFG library for use in ASIP customization”.
Alan Levicki	Summer 01	“Investigating template-aware instruction scheduling”.
Natasha Reeves ^s	Sum & Fall 01	“Low power instruction assignments in superscalars”.
Kaushik Veeraraghavan	Spr & Sum 02	“Instruction scheduling across basic blocks on the IA-64”
Rishi Gupta	Sum & Fall 02	“Converting IA-64 assembly code into a compiler IR”
Vadim Vaynerman	Fall 02 & Spr 03	“Pointer analysis for embedded systems memory allocation”
Andrew Webber ^s	Spr 03	“Predicate-enabled code compression in VLIWs”
Itai Katz	Fall 02 & Spr 03	“Instruction scheduling across basic blocks on the IA-64.”
Thomas Kwan	Fall 02 & Spr	“Efficient software caching for embedded

	03	systems”
Boris Kilimnik	Fall 02	“SSA form for embedded system data flow analysis”
Chris Cavey	Fall 02	“Speculative instructions in a trace-scheduling compiler”
Matthew Simpson*§	Summer 03	“Low overhead data compression techniques.”
Nghi Nguyen*	Summer & Fall 03	“Predication-based instruction movement for a trace-scheduling compiler”
Brian Hayes	Fall 06 & Spr 07	“Binary re-writing for enforcing security.”
Chun Cheung	Spr07	“Memory allocation for wireless sensor network nodes”
Mike Malloy	Summer 07 (ISR REU)	“Writer design and implementation for a binary rewriting software.”
Matt Randolph	Fall 08	“Derive information about Instruction and Data Cache Misses for ARM binaries through profiling.”
Rantao Chen	Fall 08	“Dynamic Profiling of X86 code to obtain information on the timing and frequencies of Basic Blocks.”
Nathan Giles	Spring 09	“Code discovery using profiling to aid binary disassembly.”

* These two students later decided to join my research group as graduate students.

§ These four students earned co-authorships on refereed conference or journal publications for the research they did as undergraduates under my supervision.

Graduate students

MS Thesis graduated under my supervision

<i>Student</i>	<i>Graduation date</i>	<i>Title of thesis</i>	<i>First employment after graduation</i>
Zhang Yi	May 02	“Execution History Guided Instruction Prefetching”	Actuate Corp., San Francisco, CA.
Oren Avissar	July 02	“An Optimal Memory Allocation Scheme for Scratch-Pad Based Embedded Systems”	Symantec Inc., Alexandria, VA
T Vinod Gupta	Aug 02	“Multi-Objective Design Space Exploration using Compiler Predictions”	TeamF1 Inc., Fremont, CA
Surupa Biswas	August 04	“Memory Overflow Protection for Embedded Systems using Run-time Checks, Reuse and Compression”	Microsoft Corp., Redmond, WA.
Bhuvan Middha	May 06	“MTSS: Multi-Task Stack Sharing for Embedded Systems.”	Microsoft Corp., Redmond, WA.
Nghi	April 07	“Memory Allocation for Embedded Systems with a	Microsoft Corp.,

Nguyen		Compile-Time Unknown Scratch-Pad Size.”	Redmond, WA.
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Ph.D Thesis graduated under my supervision

<i>Student</i>	<i>Graduation date</i>	<i>Title of thesis</i>	<i>First employment after graduation</i>
Steve Haga	October 2005.	“Reducing Code Size by Instruction Scheduling for VLIWs Based on Optimal Approaches”	Instructor, University of Pennsylvania, Erie
Sumesh Udayakumaran	May 2006	“Compiler-Decided Dynamic Memory Allocation for Scratch-Pad Based Embedded Systems”	Intel Corp, Santa Clara, CA.
Angel Dominguez	Jan 2007	“Heap Data Allocation to Scratch-Pad Memory in Embedded Systems.”	Dealeron Inc.

Graduate students for whom I am currently the advisor:

<i>Student</i>	<i>Degree Objective</i>	<i>Expected graduation date</i>	<i>Form of support</i>
George Caragea	Ph.D	2010	GRA
Alexandre Tzannes	Ph.D	2010	GRA
Matthew Simpson	PhD	2009	GTA/ Paid research staff
Matthew Smithson	PhD	2010	Employer/Self
Greeshma Yellareddy	PhD	2013	GRA
Aparna Kotha	PhD	2012	GRA
Kapil Anand	PhD	2012	GRA
Preetham Nosum	PhD	2013	Employer
Abhishek Joshi	MS	2011	GRA
Padraig O’Sullivan	MS (thesis)	2010	GRA

g. Thesis committees

*In the lists below, I have **not** included committees for students for whom I was the primary research advisor at the time of the committee.*

M.S Thesis Defense committees

Gautham T. Dorai, Anna Secka, Dorit Naishlos, Mukul Khandelia, Joseph Nuzman, Pei Gu, Yashwanth H.

M.S Scholarly paper committees

Tom Carley, Gregory Miller.

Ph.D thesis committees

Mehrdad Hassani, Nitin Chandrachoodan, Dongkeun Kim, Aamer Jaleel, Vida Kianzad, Ming-Yung Ko, Xiangrong Zhou

Ph.D proposal committee

Mehrdad Hassani, Nitin Chandrachoodan, DongKeun Kim, Aamer Jaleel, Vida Kianzad, Ming-Yung Ko, Xiangrong Zhou, Abdel-Hameed Badawy, Xin Wang, Wanli Liu

PhD Oral Qualifying examination committee

Omkar Dandekar, Chenjie Yu

4. Service

a. Scholarly Service

- Panel member, NSF Information Technology Research (ITR) Program review panel (May 2002).
- Program Committee Member, ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems (CASES), Grenoble, France. (June 2002).
- Session Chair, ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems(CASES), Grenoble, France. (October 2002).
- Panel member, NSF Sensor networks program review panel (May 2003)
- Book Reviewer for forthcoming 2nd edition of “Introduction to Logic Design” by Alan B. Marcovitz, McGraw Hill Publishers. (May 2003).
- Program Committee Member, 6th Annual IEEE Workshop on Workload Characterization (WWC-6), Austin, Texas. (September, 2003).
- Workshops Chair for workshops associated with ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems(CASES), Washington, DC. (September 2004). (Three workshops were organized).
- Program Co-Chair, 2nd workshop on Compilers and Tools for Constrained Embedded Systems (CTCES), Washington, DC. (September 2004).
- Panel member, NSF Embedded and Hybrid Systems program review panel (March 2005)
- Program committee member, ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems, Chicago, Illinois, June 15-17, 2005.
- Session Chair, ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems, Chicago, Illinois, June 15-17, 2005.

- Session Chair, ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems(CASES), San Francisco, CA, September 25-27, 2005.
- Program committee member, The Fifteenth ACM/IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT), Seattle, Washington, September 16-20, 2006.
- Program committee member, International Conference on High Performance Embedded Architectures & Compilers (HiPEAC), Ghent, BELGIUM, January 29-30, 2007.
- Session Chair, ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems(CASES), Salzburg, Austria, October 1-5 2007.
- Program committee member, ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems(CASES), Atlanta, GA, October 2008.

- Referee for several journals, including:

ACM Transactions on Embedded Computing Systems (TECS)
 IEEE Transactions on Computers (TOC)
 ACM Transactions on Computer Systems (TOCS)
 Journal of Parallel and Distributed Computing (JPDC)
 IEEE Parallel and Distributed Technology Journal
 ACM Transactions on Computer Architecture & Code Optimization (TACO)
 IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
 ACM Transactions for Programming Languages and Systems (TOPLAS)
 ACM Transactions on Software Engineering (TSE)
 ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)

- Referee for several conferences, including:

ACM Conference on Compilers, Architecture, & Synthesis for Embedded Systems (CASES)
 ACM/IEEE Conference on Parallel Architectures and Compilation Techniques (PACT)
 IEEE International Symposium on Computer Architecture (ISCA)
 ACM Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
 ACM/IEEE International Symposium on Microarchitecture (MICRO)
 IEEE/ACM/IFIP International Conference on Hardware-Software Codesign & System Synthesis (CODES+ISSS)
 ACM Conference on Languages, Compilers & Tools for Embedded Systems (LCTES)
 IEEE International Conference on Computer-Aided Design (ICCAD)
 EDA/IEEE Conference on Design Automation and Test in Europe (DATE).
 IEEE International Parallel Processing Symposium (IPPS)

b. Campus.

ECE Department

- Participated in telemarketing to admitted freshmen to try to convince them to join the university and to answer their questions. (2000, 2001, 2004 and 2007).
- Host for several faculty candidates (2000-2004).
- Member, ECE Facilities and Services Committee (2001-2003).
- GSRC Extra evaluator of applications for graduate study. (February 2002).
- Initiated and moderated discussion on proposed re-organization of the department for both teaching and research during two department retreats (Summer 2002).
- ECE salary committee (2002-2004).
- Member, Curriculum Revision Committee for EE and CE curricula, (2003-2004).
- Supervisor and mentor for several undergraduate interns through the NSF-sponsored MERIT program (2000, 2001, and 2003).
- Conducted Lab Tours of SCAL laboratory, which I co-direct, for prospective University of Maryland undergraduates students during Academically Talented Open House (Sept 6, 2003), Visit Maryland (Oct 13, 2003) and Maryland tour (April 16, 2004) events.
- Member, Faculty search committee (2003-2004).
- Chair, Course Oversight Committee for ENEE 350H. (2005).
- Member, ECE Graduate Studies and Research Committee (GSRC) (2005-2007).
- Member, Student award selection committee, 2009. This committee chose the awardees for at least three rounds of graduate student research awards, including DDF, FF and ARCS awards. Reviewed 23 detailed graduate student applications.
- Member, Human Relations and Welfare committee (2008-2010).
- Member, APT sub-committee for Computer Engineering faculty (2009).

Institute for Systems Research

- Member, ISR Facilities and Services Committee (2001-2002).

- Supervisor and mentor for two summer undergraduate intern through ISR's REU program (2002 and 2007).
- Member, ISR Salary Committee (2002-2003).
- Chairman, ISR Facilities and Services Committee (2002-2003). During my stint as chairman, the committee accomplished the following activities, among others:
 - Reviewed policies on space assignment in ISR.
 - Decided to convert AVW 3180 to a shared student space.
 - Approved the purchase of new lockers for AVW 2140 based on student feedback.
 - Asked the appropriate staff member to replace old posters in ISR spaces with newer ones.
 - Worked with a few faculty members to see if students could be permanently assigned to their research laboratories to alleviate the space shortage in ISR.
- Participant, half-day ISR strategic retreat (2005). Contributed to discussion on state of ISR and suggestions to improve it.
- Member, ISR Educational Program Committee (2006-2008). In this committee, we worked on producing an entirely new structure and curriculum for the new ISR Master of Science in Systems Engineering (MSSE) degree. We discussed goals, class timings, course sequences and course syllabi in great detail over many meetings. As a result of the committee's work, a new MSSE degree curriculum was launched in Fall 2008.
- Member, ISR Salary Committee (2008-2009).

College of Engineering

- Participant, two-day college of engineering strategic retreat (2000). Retreat composed of a series of two-hour focus groups on creating and sustaining excellence in the Clark School of Engineering.
- Presented a lecture in "Dialog with the Dean" class on October 16, 2002, titled "An Overview of Embedded Systems". This is a class of engineering freshman, and the lectures aim to provide a view of innovative ongoing research at the University.
- Faculty Mentor, Inventis Program. (2007-2008) Intensively mentored three undergraduate students via several meetings per semester.
- ECE representative, University of Maryland Energy Research Center (UMERC) Faculty search committee (2007-2008). We reviewed hundreds on applications, and invited eight candidates to interview to fill three positions.

University

- Invited lecture in “The Student in the University” class (UNIV 100) on November 6, 2003. This is a freshman orientation course for engineering majors. My lecture overviewed careers and technical content in Computer Engineering.