

**Digital Logic – Ph.D. Qualifying Exam August 2009**

**(i) (6 pts.)**

Implement the full adder circuit using 2 x 1 multiplexers. You can use Boolean constants 0 and 1 in your design if you like.

**(ii) (7 pts.)**

Design a 3 x 8 decoder with enable using 1 x 2 decoders with enable.

**(iii) (7 pts.)**

Design a circuit that uses only a T flip-flop and standard logic gates to perform the following operation:

Given a one bit input  $x$ . If  $x = 0$  then the data in the T flip-flop becomes 0 at the rising clock edge. If  $x = 1$  then the data in the T flip-flop becomes 1 at the rising clock edge.

Show work.