

Devices – Ph.D. Qualifying Exam Fall 2009

(i) (6 pts.)

- a) (3 pts) Suppose you have a planar p-n junction with an acceptor concentration $N_A = 10^{16} \text{cm}^{-3}$ on the p-side and a donor concentration $N_D = 3 \times 10^{16} \text{cm}^{-3}$ on the n-side. If the depletion width on the N-side is $x_n = 0.087 \mu\text{m}$, what is the depletion width on the P-side?
- b) (3 pts) There is an electric field in the depletion region of a PN junction, yet no external current would flow if you were to connect a wire from the N-side to the P-side of the junction. Why?

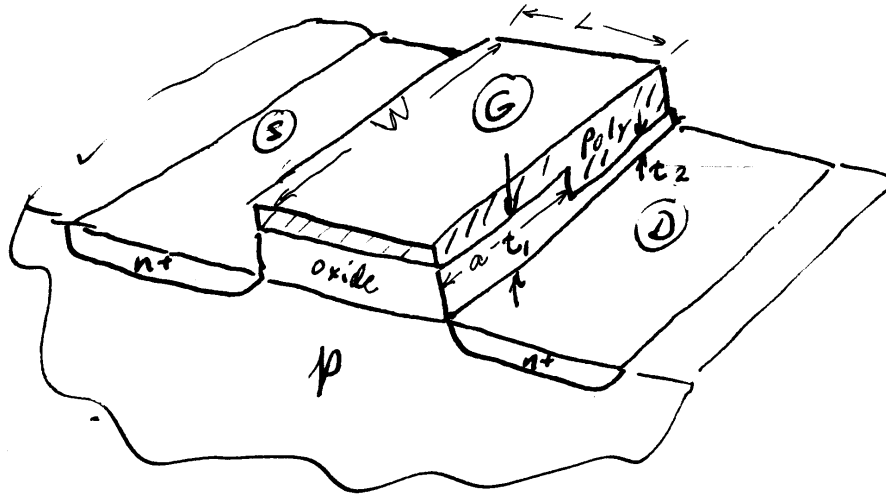
(ii) (7 pts.)

The characteristic, (i.e. drain-source current, I_{DS}) of an ideal MOSFET in saturation as a function of gate source voltage, V_{GS} and threshold voltage, V_T (which depends on various transistor parameters), is

$$I_{DS} = (K/2)(V_{GS} - V_T)^2 \quad \text{where } K = (W/L)\mu_e(\epsilon_{ox}/t_{ox})$$

where μ_e is the electron mobility, ϵ_{ox} is the dielectric constant of the oxide.

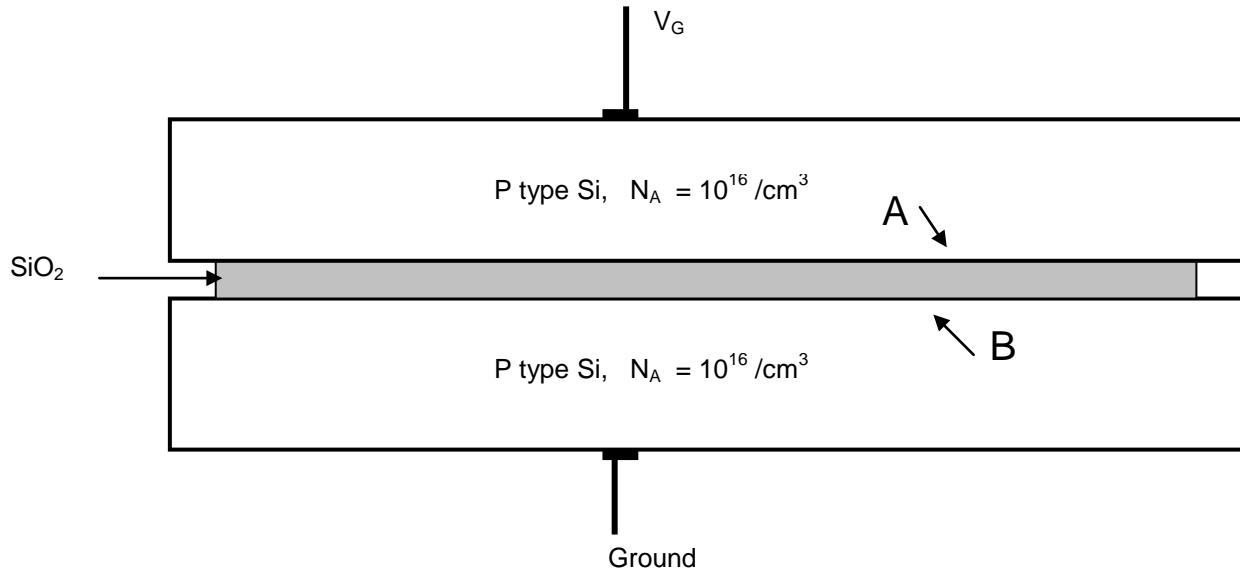
Suppose you have an nMOS transistor whose gate oxide thickness, t_{ox} , changes from t_1 to t_2 in the middle of the channel width as shown in the figure below.



- a) (3pts) How would you expect this transistor to behave. In particular, how would the plot of $(I_{DS})^{1/2}$ vs. V_{GS} at constant V_{DS} (in saturation) look? Identify key features.
- b) (4pts) Given the saturation characteristics of an ideal MOSFET above, write down an expression for I_{DS} (in saturation) for the nMOS transistor shown above

(iii) (7 pts.)

The structure shown below made up of an oxide layer 10nm thick sandwiched between two *identical* p-type silicon layers. Consider the problem to be one dimensional, i.e. the structure is large in the horizontal direction and in the direction out of the paper.



- a) (3pts) Sketch qualitatively the small signal (or AC) capacitance measured from the top contact to ground versus V_G as V_G is varied from $-3V$ to $+3V$, i.e. sketch the CV characteristic from $-3V$ to $+3V$. (the AC capacitance to ground measured as you apply a DC voltage to the top contact) You don't have to calculate any values but identify key features on the sketch.

- b) (4pts) If you apply a small *positive* voltage, V_G to the top contact, what is the state of the surface A in the silicon, and of the surface B? (e.g., inverted, accumulated, depleted, or unchanged from the bulk Si). Explain, don't just guess.