

# PhD Qualifier Exam, Spring 2006

## Computer Architecture and Systems

1. (6 points) Consider an assembly-level architecture, with its own assembly language. If a new instruction is added to this assembly-level architecture, explain in detail the change(s) that should be made (if at all) to:
  - (a) the compiler (high-level language  $\rightarrow$  assembly language translator)?
  - (b) the assembler (assembly language  $\rightarrow$  machine language translator)?
  - (c) the CPU control unit (machine language  $\rightarrow$  microinstruction interpreter)?
  
2. (6 points) Explain (with a diagram) how pipelining the processor data path helps improve performance.
  
3. (8 points) A virtual memory system uses 15-bit virtual addresses. The physical memory consists of 8 Kbytes. The page size is 2 Kbytes. The translation lookaside buffer (TLB) has 3 entries. Both the TLB and the page table are replaced using the LRU (least recently used) policy.
  - (a) (2 point) Indicate using a diagram how the memory management unit (MMU) would split a 15-bit address to get the virtual page number (VPN).
  
  - (b) (4 points) Consider the following sequence of memory address accesses: 0x6ffc, 0x7ffc, 0x6000, 0x4000, 0x3000, 0x2000, 0x7ffc, 0x2008, 0x74fc, 0x64fc. For each of these accesses, indicate if it would be a TLB hit or miss. Also indicate if it would be a page fault or not.
  
  - (c) (2 points) Draw the final state of the TLB and the page table.