University of Maryland Professional Masters Program  Term: Fall 2004
Course No.: ENPM 607  Course Title: Computer System Design and Architecture
INSTRUCTOR: Dr. Charles B. Silio
ADDRESS: Electrical and Computer Engineering Department
University of Maryland
College Park, MD 20742-3285

Phone: 301-405-3668  E-Mail Address: silio@eng.umd.edu

Office Hours: UMCP: Wednesday 2:00–3:50 p.m., Monday & Friday 11:00 a.m.–12 noon
Course Day/Time Meet: Wednesday 4:00 p.m.–5:15 p.m. & 5:25 p.m.–6:40 p.m.

Texts: (2 both Required)

Principal References:

Prerequisites: An undergraduate course in Computer Organization, Introduction to Computer architecture, or equivalent.

Course outline:

1. Principles of computer design; cost/performance of design options;
2. Processor design: instruction set design and implementation; pipelining; floating-point arithmetic;
3. Memory-Hierarchy design: caches; main memory design (e.g., interleaving); virtual memory; performance analysis;
4. Input/Output design: I/O performance measures, types of I/O devices, I/O device connection to CPU/Main Memory;
5. Parallel system design; SIMD, MIMD, and SPMD architectures
6. Interconnection networks for processors and memories
7. Pipeline optimizations, superscalar processor architectures.

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Course Description:

This course is intended to cover modern computer system designs and architectures. The first part of the course will focus on principles of computer design and cost/performance factors; instruction set design and implementation, RISC vs. CISC instruction sets; control unit and pipeline design; floating-point arithmetic; memory hierarchy designs, caches, memory interleaving, virtual memory; I/O device interconnections to CPUs and main memory.

The second part of the course will cover advanced computer architectures. These include parallel system designs, SIMD, MIMD, SPMD; interconnection networks for processors and memories; optimization of pipeline operations; superscalar architectures.

The course will rely on examples of real, commercially available, systems to illustrate the concepts presented in class. These shall include one or more of the MIPS architectures, DEC-Alpha series, PowerPC, Intel 80x86 series and IA-64. Examples shall also include one or more of Cray MP architectures, Thinking Machines' CM-5, Kendall Square Research KSR-1.

Course Requirements:

Exams: 3 equally weighted (75 min.) exams; 3rd exam on last class day: Dec. 8, 2004.

Grading:

Exam 1 (Tentative Date: Oct. 13) 33\(\frac{1}{3}\)%

Exam 2 (Tentative Date: Nov. 10) 33\(\frac{1}{3}\)%

Exact dates to be announced by instructor later.

Exam 3 (Firm Date: December 8) 33\(\frac{1}{3}\)%

Homework (Textbook readings and readings of articles from the technical literature, and assigned problems some of which are similar to exam problems)