Course Syllabus

ENEE 759M: Advanced Topics in Microarchitecture, Spring 2000
Prof. Bruce Jacob

1. Basic Information

Time & Place

Lecture: TuTh 2:00-3:15, EGR-1104

Professor

Bruce L. Jacob: AVW-1325, blj@eng.umd.edu
Office hours: Tuesday 3:15–4:30, Wednesday 1:00–2:30

Class Home Page

http://www.ee.umd.edu/courses/enee759m/

Class Email List

enee759m-01@coursemail.umd.edu

Class Schedule

Office hours are subject to change; changes will be announced in class.

<table>
<tr><th></th><th>Mon</th><th>Tue</th><th>Wed</th><th>Thu</th><th>Fri</th></tr>
<tr><td>10-10:30</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>10:30-11</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>11-11:30</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>11:30-12</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>12-12:30</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>12:30-1</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>1-1:30</td><td rowspan="4">GSRA Meetings</td><td></td><td rowspan="3">Instructor Office Hours</td><td></td><td></td></tr>
<tr><td>1:30-2</td><td></td><td></td><td></td></tr>
<tr><td>2-2:30</td><td rowspan="3">Lecture (EGR-1104)</td><td rowspan="3">Lecture (EGR-1104)</td><td></td></tr>
<tr><td>2:30-3</td><td></td><td></td></tr>
<tr><td>3-3:30</td><td rowspan="3">CE Colloquium (AVW-2460)</td><td></td><td></td></tr>
<tr><td>3:30-4</td><td rowspan="2">Instructor Office Hours</td><td></td><td></td><td></td></tr>
<tr><td>4-4:30</td><td></td><td></td><td></td></tr>
<tr><td>4:30-5</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>5-5:30</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>5:30-6</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

2. Course Overview

This course covers advanced topics in the architecture and design of microprocessors, memory hierarchies, and system-level software. We will read some recent papers on cutting-edge research as well as some of the more influential papers in computer architecture—you will notice that many of these papers have been around for several decades, but the topics they cover are highly advanced nonetheless. In fact, many of the techniques used in today's high-performance superscalar processors were invented in the 1960's and "rediscovered" only in the last decade.

We will also discuss the methodologies, mechanisms, and tools used by researchers in the field of architecture. You will become familiar with these over the course of the semester by working on a research project which will count for 40% of your grade.

3. Prerequisites

Students should understand the fundamentals of **caches**, **pipelines**, and **processor organization**. This means you should understand *how* they work as well as *why* they work.

4. Course Material

There is one required text for the course—a collection of selected papers published by Morgan Kaufmann:

> *Readings in Computer Architecture*, by Mark Hill, Norm Jouppi, and Guri Sohi (eds). Morgan Kaufmann, 2000.

This is a (far from complete) collection papers that you really should read if you intend to pursue computer architecture. We will cover anywhere from two to four papers per week from the textbook. Unfortunately, there are too many papers to cover in a single 3-hour semester course, so we will probably cover a bit more than half the book. The textbook will be supplemented from time to time by additional papers that I provide.

There are several recommended textbooks that you might find useful, and which give a decent amount of background and insight into the advanced topics. The first is Mike Johnson's thesis and contains a brief description of how one could create a superscalar implementation of the x86 ISA (remember that this thesis was written several years before the Pentium—the first superscalar x86—was introduced). The second is by one of the best researchers in the field, Jim Smith, and it is more advanced and more clearly written than Johnson's book. The last is more recent (four years in the computer industry is an eternity), and it presents a study of the AMD K6 architecture.

> *Superscalar Microprocessor Design*, by Mike Johnson. Prentice Hall 1991.
>
> *POWER and PowerPC*, by Shlomo Weiss and James E. Smith. Morgan Kaufmann 1994.
>
> *The Anatomy of a High-Performance Microprocessor*, by Bruce Shriver and Bennett Smith. IEEE Computer Society Press, 1998.

You are not required to purchase or read these last three books; however, they serve as good background reading and can help bring you up to speed on most of the concepts covered in this course. Should you pursue computer architecture, you will likely want them on your bookshelf.

5. Course Work, Policies, and Grading

There will be a midterm exam, a final exam, and a final project. The exams will be based entirely on the course readings and will be closed book, closed notes. They will both follow this format: I will give you 12 questions a week before the exam. On the day of the exam, I will ask you four or five of the 12 questions. They will be essay questions, of course. You are encouraged to collaborate in your preparation for the exams. Similarly, you may collaborate on your projects.

Final grades will be based on the total of points earned on the project and exams. The tentative point breakdown is as follows:

Project: 40%

Midterm Exam: 30% (March 16, in class)

Final Exam: 30% (May 20, 10:30-12:30)

Note: This is a graduate-level class; I expect graduate-level work. I expect you to read the papers in preparation for lecture and to participate in the discussions. I expect you to start your research project early enough that you can finish it by the end of the term. I expect you to prepare thoroughly for the exams.

6. Lecture Schedule

Here is the tentative order for the semester's lectures, which roughly corresponds to the topical sections in the coursepack—in an order that presents some meaty topics early so that you have a good preparation for your research project. Final projects will be due at the end of the semester; you will turn in a research report (a paper) and give a 10-minute presentation on the work.

Week of	Subject
Jan. 31	Intro to course Architecture primer: caches, pipelining, processor organization
Feb. 7	Instruction-level parallelism: VLIW, superscalar design, limitations
Feb. 14	Dynamic scheduling & out-of-order execution
Feb. 21	Out-of-order pipelines and precise interrupts
Feb. 28	Advanced cache topics
Mar. 6	Primary memory systems
Mar. 13	**Review & Midterm** (March 16, in class)
Mar. 20	**Spring Break**
Mar. 27	Branch prediction and data prediction
Apr. 3	Low-power architecture design **Research abstract** due April 6, in class
Apr. 10	Hardware/software interaction
Apr. 17	Memory management
Apr. 24	Recent paradigm shifts: multiscalar, SMT, CMP, EPIC
May 1	Historical case studies
May 8	**Project Presentations** (May 9 & 11, in class)
May 15	Future trends
Exams	**Final Exam** — May 20, 10:30-12:30

7. Special Needs

If you have a documented disability that requires special needs, please see me as soon as possible, and certainly no later than the third week of classes.