SDRAM, DDR SDRAM and DDR2 SDRAM Memory Systems

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Memory System Topology

Single Channel SDRAM Controller

“Mesh Topology”

- Blue: Addr & Cmd
- Red: Data Bus
- Green: Chip (DIMM) Select
SDRAM Chip Basics

**66, 100, 133 MHz**

**Multiplexed Address Bus**

**Programmable Burst Length, 1,2,4,8 or page**

**Quad Banks Internally**

**Supply Voltage of 3.3V**

**Low Latency, CAS = 2, 3**

**LVTTL Signaling (0.8V to 2.0V)**

**(0 to 3.3V rail to rail.)**

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<table>
<thead>
<tr>
<th>Condition Specification</th>
<th>Cur.</th>
<th>Pwr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating (Active) Burst = Continuous</td>
<td>300mA</td>
<td>1W</td>
</tr>
<tr>
<td>Operating (Active) Burst = 2</td>
<td>170mA</td>
<td>560mW</td>
</tr>
<tr>
<td>Standby (Active) All banks active</td>
<td>60mA</td>
<td>200mW</td>
</tr>
<tr>
<td>Standby (powerdown) All banks inactive</td>
<td>2mA</td>
<td>6.6mW</td>
</tr>
</tbody>
</table>
SDRAM Chip Architecture

256 Mbit chip: 8192 rows, 512 columns, x16 data, 4 banks
Mode Register

SDRAM Device can be programmed to respond in slightly different manners.
# Command Truth Table

<table>
<thead>
<tr>
<th>Command Description</th>
<th>CS#</th>
<th>RAS#</th>
<th>CAS#</th>
<th>WE#</th>
<th>DQM</th>
<th>addr</th>
<th>DQs</th>
</tr>
</thead>
<tbody>
<tr>
<td>command inhibit (nop)</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>no operation (nop)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>active (activate row - RAS)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>addr</td>
<td>X</td>
</tr>
<tr>
<td>read (start read - CAS)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L/H</td>
<td>addr</td>
<td>X</td>
</tr>
<tr>
<td>write (start write - CAS W)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L/H</td>
<td>addr</td>
<td>valid</td>
</tr>
<tr>
<td>burst terminate</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>active</td>
</tr>
<tr>
<td>precharge</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>**</td>
<td>X</td>
</tr>
<tr>
<td>auto refresh</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>load mode register</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>code</td>
<td>X</td>
</tr>
<tr>
<td>write enable/output enable</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>H</td>
<td>-</td>
<td>active</td>
</tr>
<tr>
<td>write disable/output High-Z</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>L</td>
<td>-</td>
<td>hi-Z</td>
</tr>
</tbody>
</table>

** bank address, or all banks with a_10 assertion
System Initialization

1. Apply power to Vdd and VddQ
2a. Wait 100us before issuing command to DRAM chip
2b. Read out SPD
3. Issue at least one NOP
4. Issue precharge-all command
5. Issue two auto-refresh commands
6. Program mode register
CAS Read/Write Commands

- **Read Command**
  - Command bus
  - DQ (data bus)
  - CAS = 2
  - \( t_{OH} \)
  - D out

- **Write Command**
  - Command bus
  - D in
  - DQ (data bus)
  - CAS = 3
  - \( t_{OH} \)
Piplined CAS Reads

Memory Controller
SDRAM rank # 0
SDRAM rank # 1

Clock signal
Data bus
Data return from rank # 0
Data return from rank # 1

rank # 0 hold time
bus idle time
rank # 1 setup time

data bus utilization
read command and address assertion
CASL 3

0 1 2 3 4 5 6 7 8 9 10 11 12 13

Data bus
Write after Read

Clock signal

Data bus

Data return from rank #0

Data written from memory controller

bus idle time

rank #0 hold time

setup time

bus idle time

setup time

Memory Controller

SDRAM rank #0

SDRAM rank #1
Read after Write

Back-to-back accesses to same rank

Back-to-back accesses to different ranks

Memory Controller
SDRAM rank # 0
SDRAM rank # 1
Data bus

write command
read command
CASL = 3

write command
read command
CASL = 3
Multiplexed Address Bus

- Active command bus read
- Row address
- Address bus
- Column address
- \( t_{\text{RAS}} = 3 \)
- Mode register
- Address register
- Row address mux
- Bank control logic
- Column address counter/latch
Signaling: LVTTL

- No reference voltage
- Rail-to-rail swing of 3.3V

V_{in} low = 0.8V  V_{in} high = 2.0V

V_{out} high = 2.4V  V_{out} low = 0.4V

Vin

1.0

2.0

3.0

3.3

V_{out}

LVTTL inverter

input voltage

output voltage
DDR SDRAM Memory System

Same Topology as SDRAM
DDR SDRAM Chip

- 100, 133, 166, 200 MHz (200, 266.. etc Mbps)
- Multiplexed Address Bus
- Programmable Burst Lengths, 2, 4 or 8*
- Quad Banks Internally
- Supply Voltage of 2.5V*
- Low Latency, CAS = 2, 2.5, 3 *
- SSTL-2 Signaling (Vref +/- 0.15V)
- (0 to 2.5V rail to rail)

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Diagram:
- Clk #
- Clk
- Cmd
- DQS
- Data
- CASL = 2
- DQS Post-amble
- DQS Pre-amble

Chip:
- 256 MBit
- 66 pin
- TSOP

Pinouts:
- 16 Pwr/Gnd*
- 16 Data
- 15 Addr
- 7 Cmd
- 2 Clk *
- 7 NC *
- 2 DQS *
- 1 Vref *
DDR SDRAM Chip

Same basic architecture as SDRAM

Data I/O runs at 2X freq. of DRAM core

Data I/O Interface is different

Same basic architecture as SDRAM

Data I/O runs at 2X freq. of DRAM core

Data I/O Interface is different
Signal Propagation

Ideal Transmission Line

~ 0.66c = 20 cm/ns

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line
Clocking Issue

**Figure 1:**
Write Data

**Figure 2:**
Read Data

We need different “clocks” for R/W
DQS: Data Strobe

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- Single ended, bidirectional signal in DDR SDRAM memory system
DQS: Read and Write

Read

Write
DQS: Read-Read Sequence

DQS pre-amble

DQS post-amble

Clk #  
Clk

Cmd  
\( r_0 \)  
\( r_1 \)

DQS

Data

\( d_0 d_0 d_0 d_0 \)  
\( d_1 d_1 d_1 d_1 \)

CASL = 2
Signaling: SSTL-2

- $V_{\text{ref}} = V_{\text{ddq}}/2$
- Rail-to-rail swing of 2.5V

$V_{\text{in low}} = V_{\text{ref}} - 0.15v$
$V_{\text{in High}} = V_{\text{ref}} + 0.15v$

$V_{\text{out low}} = V_{\text{ddq}} - 0.373V$
$V_{\text{out low}} = 0.373V$

SSTL-2 output voltage inverter

$V_{\text{in}}$, $V_{\text{out}}$, input voltage, output voltage
DDR SDRAM Quick Summary

- Same basic architecture as SDRAM
- DQS added to better control timing of data transport
- Single-ended, bi-directional DQS signal reduces “efficiency” of access protocol
- Single-ended, bi-directional DQS signal very difficult to turn around on system board level @ 200 MHz
- Data accessed in 2n widths @ frequency m internally and n width @ frequency 2m externally
- Voltage supply dropped to 2.5V, lower power consumption
DDR II Memory System

Same Topology as DDR SDRAM

Single Channel DDR II SDRAM Controller

DIMM1

Rank1  Rank2

DIMM2

Rank1  Rank2

DDR II Memory System

Single Channel DDR II SDRAM Controller

 Addr & Cmd

 Data Bus

 Differential DQS

 Chip (DIMM) Select
DDR II SDRAM Chip Basics

- 200, 266, 333 MHz $f_{ck}$ (400, 533, 667 Mbps)
- Multiplexed Address Bus
- Programmable Burst Length 4, 8
- Quad Banks Internally (1+ Gb: 8 banks)
- Read Latency, CAS = 3, 4, 5
- Write Latency, WL = CL - 1
- Posted CAS
- Additive Latency, AL = 0, 1, 2, 3, 4, 5
- Differential Data Strobe
- Supply Voltage of 1.8V (2.5V optional)
- SSTL_18 Signaling ($0.5*V_{ddq} \pm 0.1V$)
- (0 to 1.8V rail to rail.)
- Programmable I/O Drive Strength
- On Die Termination

10 Vdd/Gnd I/O
8 Vdd/Gnd Core
2 Vdd/Gnd DLL
17 Addr
8 Data
4 DQS
2 Clk
1 Vref
2 NC
6 Cmd (CS#, CAS#, WE#, CKE, ODT, RAS#)

x8 chip pin definition

- x4, x8
  - 60 ball FBGA
- x16
  - 84 ball FBGA
DDR II Chip Architecture

Same basic architecture as SDRAM & DDR SDRAM (+Hardware for Posted CAS)
Data I/O runs at 4X bit rate of DRAM core

Data I/O Interface is different

ODT control clk OCD control

read latch MUX

write FIFO and drivers

MUX

output drivers & ODT

input buffer

DQS I/O Buffer

clk

data bus (and mask)
Recall: “DRAM Evolution”

- Cost adder:
  - 5%

Dominant DRAM Generation:
- 16Mbit:
  - DDR SDRAM
  - 200 Mbp/s/p
- 64Mbit:
  - SDRAM
  - 400 Mbp/s/p
- 256Mbit:
  - SDRAM
  - 800 Mbp/s/p
- 1Gbit:
  - {DDR2}
  - {RDRAM}
  - >1 Gbp/s/p

- Internal datapath width (16 bit external I/O):
  - x16
  - x32
  - x64
  - x128
  - x256

Years:
- 1995
- 1998
- 2001
- 2004
- 2007
Mode Registers

SDRAM, DDR SDRAM & DDR II SDRAM Devices can be programmed to behave in slightly different manners.
Posted CAS (Read)

CAS command follows RAS command. (AL = 0)

\[ t_{RL} = t_{CAS} + t_{AL} \]

1. RAS: Row Access
2. CAS: Column Read Access
Posted CAS (Write)

CAS Write follows RAS. ($t_{AL} = 0$, $t_{WL} = 2$)

$\begin{align*}
\text{t}_{WL} &= \text{t}_{CAS} + \text{t}_{AL} - 1 \\
\text{t}_{AL} &= \text{t}_{WL} = \text{t}_{CAS} + \text{t}_{AL} - 1
\end{align*}$

1. RAS: Row Access
2. CAS: Column Write Access
Write after Read (same rank)

- **ck#**
- **ck**
- **cmd**
  - 1
  - 2
  - 4
  - 2
- **data**
- **dqs#**
- **dqs**

**t_{AL} (Additive Latency)**

**t_{RL}**

\( t_{AL} = 2, \ t_{CAS} = 3 \)

1. RAS: Row Access
2. CAS: Column Read Command
3. CAS: Column Read Data
4. CAS: Column Write Command
5. CAS: Column Write Data

\[
\begin{align*}
 t_{RL} &= t_{CAS} + t_{AL} = 3 + 2 = 5 \\
 t_{WL} &= t_{CAS} + t_{AL} - 1 = t_{RL} - 1 = 4
\end{align*}
\]
Read after Write (same rank)

1. RAS: Row Access
2. CAS: Column Write Command
3. CAS: Column Write Data
4. CAS: Column Read Command
5. CAS: Column Read Data

\[ t_{RL} = t_{CAS} + t_{AL} = 3 + 2 = 5 \]
\[ t_{WL} = t_{CAS} + t_{AL} - 1 = t_{RL} - 1 = 4 \]
Recall: DQS in DDR SDRAM

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- Single ended, bidirectional signal in DDR SDRAM memory system
- One signal per byte
DQS in DDR II

- Topology, electrically matched with signals on data bus
- Source synchronous “clock” signal
- Edge aligned with data for reads, center aligned with data for writes
- **Differential**, bidirectional signal in DDR II memory system
Signaling: SSTL-18

- $V_{\text{ref}} = V_{\text{ddq}}/2$
- Rail-to-rail swing of 1.8V

$V_{\text{in low}} = V_{\text{ref}} - 0.125v$
$V_{\text{in High}} = V_{\text{ref}} + 0.125v$

$V_{\text{out hi}} = V_{\text{tt}} + 0.603V$
$V_{\text{out low}} = V_{\text{tt}} - 0.603V$
Impedance Topology I

-Recall: If
  
  $Z_{\text{out}} \gg Z_0$, current mode.
  
  $Z_{\text{out}} \ll Z_0$, voltage mode
Impedance Topology II

Controller

Write

Read

Z_{out} -> terminate

Z_{0}
ODT: On Die Termination

- Controlled by memory controller via ODT pin.
- Can be turned on/off in 2 cycles
- Provides active termination at the receiver interface.
ODT Control for Read

- **ck#**
- **ck**
- **cmd**
- **data**
- **dqs#**
- **dqs**
- **ODT turn on delay**
- **ODT turn off delay**
- Controller
- **Z_{out}**
- **Z_0 -> terminate**
DDR II Quick Summary

- Same basic architecture as DDR SDRAM
- Optional DQS and RDQS (RDQS) added to better control timing of data transport
- Data accessed in 4n widths @ frequency m internally and n width @ frequency 4m externally
- DRAM Core and I/O voltage supplies dropped to 1.8V, 2.5V retained in spec for use with DDR SDRAM compliant system designs
- Dynamic termination control
- Edge rate calibration/control