Memory System Organization

Credit where credit is due:
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Memory System Organization

Single Channel SDRAM Controller

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Dimm1  Dimm2  Dimm3  Dimm4
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"Mesh Topology"

- Addr & Cmd
- Data Bus
- Chip (DIMM) Select

University of Maryland ECE Dept.
Where is the data?

CPU

Request (Read)
(Physical Address)
(Cacheline length = 64B)

Data

Magic
Memory
Controller

Data

Command
Sequence

Rank Address = ?
Bank Address = ?
Row address = ?
Column Address ?
Channel I

“Typical” memory system.
1 physical channel of DDR SDRAM

Intel i850 system controller

Intel i875P system controller

Intel i850 DRDRAM memory system.
2 physical channel. 1 logical channel

Intel 875P DDR SDRAM memory system.
2 physical channel. 1 logical channel
Channel II

Two Channels: 64 bit wide per channel

Compaq Alpha EV7 processor
DMC
DMC

Intel i925X system controller
DMC
DMC

D-RDRAM
D-RDRAM
D-RDRAM
D-RDRAM
D-RDRAM
D-RDRAM
DDR2
DDR2
It’s a “bank” of chips that responds to a single command and returns data.

“Bank” terminology already used.
Rank II

- Single Sided Dimm (One Rank)
- Double Sided Dimm (Two Ranks)
- Rambus RIMM
  - Rank Count is Number of Devices

SDRAM
- Single Sided Dimm (One Rank)

SDRAM/DDR SDRAM system: 1~6 ranks
RDRAM system: <= 32 ranks
“Banks” of independent memory arrays inside of a DRAM Chip

SDRAM/DDR SDRAM system: 4 banks
RDRAM system: “32” split or 16 full banks
one row spanning multiple DRAM devices

Row

DRAM devices arranged in parallel in a given rank
Column

DRAM devices arranged in parallel in a given rank

SDRAM memory systems: width of data bus = column size

Column = Smallest unit of data moved in memory system
Where’s the data? Part 1

Read Request
Physical Address: 0x0AC75C38

Magic Memory Controller

32 bit physical address (byte addressable)

Rank id = 1
Bank id = 1
Row id = 0x0B1D
Column id = 0x187
Where’s the data? Part 2

Bank id = 1

Rank id = 1

Row id = 0x0B1D

Column id = 0x187

FPM / EDO / SDRAM / etc.
Bare Chips

Bare DIP’s shoved into sockets
18 Chips, each x1, 18 bit wide data bus
Organizing chips into modules

Put chips on PCB, make a module

Data

Address

Data

FPM / EDO / SDRAM / etc.
Memory Modules II

Single Inline Memory Module
Memory Modules III

Dual Inline Memory Module

electrically different contact
Memory Modules IV

Registered DIMM

One extra cycle to buffer and distribute address.

More chips (load) can be placed on module
## Memory Modules V

<table>
<thead>
<tr>
<th>Capacity</th>
<th>device density</th>
<th>number of ranks</th>
<th>devices per rank</th>
<th>device width</th>
<th>number of banks</th>
<th>number of rows</th>
<th>number of columns</th>
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</thead>
<tbody>
<tr>
<td>128 MB</td>
<td>64 Mbit</td>
<td>1</td>
<td>16</td>
<td>x4</td>
<td>4</td>
<td>4096</td>
<td>1024</td>
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<td>64 Mbit</td>
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<td>8</td>
<td>x8</td>
<td>4</td>
<td>4096</td>
<td>512</td>
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<tr>
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<td>128 Mbit</td>
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<td>4</td>
<td>4096</td>
<td>1024</td>
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<tr>
<td>128 MB</td>
<td>256 Mbit</td>
<td>1</td>
<td>4</td>
<td>x16</td>
<td>4</td>
<td>8192</td>
<td>512</td>
</tr>
</tbody>
</table>

Four different configurations for a 128 MB SDRAM DIMM
SPD: Serial Presence Detect

SPD: Tiny EEPROM
Contains Parameters
- Speed settings
- Configurations
- Programmed by module maker
Kingston SDRAM DIMM

8 Chips. 128 Mbit each. (Infineon)

SPD

PC133

CAS 3

Dual Inline Memory Module