Alternative DRAM Devices
Market Fragmentation?

3.2 Gbps/pin pair
High Datarate  \( t_{RC} \approx 50\text{ns} \)
Low Latency  XDR
High Performance  \( t_{RC} < 20\text{ns} \)
Commodity

MoR = Mobile RAM  CeR = Cellular RAM

MoR, CeR

GDDR

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Commodity

MoR = Mobile RAM  CeR = Cellular RAM

Market Fragmentation

FPM  ➔  EDO  ➔  SDR  ➔  DDR  ➔  DDR2  ➔  DDR3
DRAM for Embedded Systems

- Relatively small memory size demand; tens of megabytes. One or two chips would provide sufficient capacity.
- No need for expandability (one/two ranks), no need for sockets, short traces.
- Examples: graphics cards, network routers, game consoles.
- Low(er) latency, high(er) cost.
- Sometimes, act as SRAM replacement.
- Diverse requirements. Graphics cards favor streaming. Network equipment favors random access of 40 byte (IP) packets or 53 byte (ATM) packets.
Candidates

- Commodity DDRx
- XDR
- Alternative Memory Technologies: NVRAM/MRAM?/FeRAM?/PCRAM?
- GDDRx
- RLDRAM I/II
- FCRAM/NetDRAM
- Cellular DRAM
- Mobile DRAM
- eDRAM
GDDR3

DDR2:
- Datarate: 400~800 Mbps
- DQS: bi-directional differential per byte
- Topology: up to 4 ranks
- Voltage: 1.8v
- Bus Width: x4 ~ x16
- \( t_{RC} \): ~55 ns
- Refresh: 64 ms

GDDR3:
- Datarate: 1.0 ~ 1.4 Gbps
- DQS: uni-directional single ended R/W per byte
- Topology: 1 rank only
- Voltage: 2.0v
- Bus Width: x32
- \( t_{RC} \): ~42 ns
- Refresh: 32 ms
RLDRAM: SRAM-like

High-end PC and Server

RLDRAM is a great replacement to SRAM in L3 cache applications because of its high density, low power and low cost

* Infineon Presentation, Denali MemCon 2002
# RLDRAM/FCRAM/DDRx

<table>
<thead>
<tr>
<th>DRAM Type</th>
<th>Datarate</th>
<th>Bus Width (per chip)</th>
<th>Peak Bandwidth (per Chip)</th>
<th>Random Access Time ($t_{RAC}$)</th>
<th>Row Cycle Time ($t_{RC}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR 400</td>
<td>200 * 2</td>
<td>16</td>
<td>0.8 GB/s</td>
<td>30 ns</td>
<td>55 ns</td>
</tr>
<tr>
<td>DDR2 667</td>
<td>333 * 2</td>
<td>16</td>
<td>1.1 GB/s</td>
<td>24 ns</td>
<td>54 ns</td>
</tr>
<tr>
<td>FCRAM</td>
<td>200 * 2</td>
<td>16</td>
<td>0.8 GB/s</td>
<td>22 ns</td>
<td>25 ns</td>
</tr>
<tr>
<td>FCRAM II</td>
<td>333 * 2</td>
<td>9 ~ 36</td>
<td>2.6 GB/s</td>
<td>&lt; 20 ns</td>
<td>&lt; 20 ns</td>
</tr>
<tr>
<td>RLDRAM I</td>
<td>300 * 2</td>
<td>32</td>
<td>2.4 GB/s</td>
<td>20 ns</td>
<td>25 ns</td>
</tr>
<tr>
<td>RLDRAM II</td>
<td>533 * 2</td>
<td>36</td>
<td>4.5 GB/s</td>
<td>15 ns</td>
<td>15 ns</td>
</tr>
<tr>
<td>XDR</td>
<td>1600 * 2</td>
<td>4 ~ 16</td>
<td>6.4 GB/s</td>
<td>35 ns</td>
<td>50 ns</td>
</tr>
</tbody>
</table>

**RL-DRAMx:** No Connectors  
**FCRAMx:** Modules Available  
**Non-Multiplexed Address? (SRAM like)**  
**Hidden Precharge? Always close-page.**
RLDRAM II

- Successor to RLDRAM
- Very much unlike DDRx
- Infineon to Micron
- Two versions: Split I/O or Common I/O

- Lower datarate than XDR, but . . .
- Supports burst length of 2.
- \( t_{\text{Burst}} = 2.5\,\text{ns}, \ t_{\text{RC}} = 20\,\text{ns} \) (@ 400 MHz)
- XDR: \( t_{\text{Burst}} = 5\,\text{ns}, \ t_{\text{RC}} = 50\,\text{ns} \)
- More “randomness”.
- “Random BW” vs “Stream BW”.
- Designed for telecommunications gear.
### Fast Cycle RAM (aka Network-DRAM)

<table>
<thead>
<tr>
<th>Features</th>
<th>DDR SDRAM</th>
<th>FCRAM (Network-DRAM)</th>
<th>FCRAM II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd, Vddq</td>
<td>2.5 +/- 0.2V</td>
<td>2.5 +/- 0.15</td>
<td>2.5 +/- 0.15</td>
</tr>
<tr>
<td>Elec. Interface</td>
<td>SSTL-2</td>
<td>SSTL-2</td>
<td>SSTL-2</td>
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<tr>
<td>Clock Freq.</td>
<td>100~200 MHz</td>
<td>154~200 MHz</td>
<td>333 MHz</td>
</tr>
<tr>
<td>t(_{RAC})</td>
<td>~40ns</td>
<td>22~26ns</td>
<td>20ns</td>
</tr>
<tr>
<td>t(_{RC})</td>
<td>~60ns</td>
<td>25~30ns</td>
<td>20ns</td>
</tr>
<tr>
<td># Banks</td>
<td>4</td>
<td>4</td>
<td>8</td>
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<tr>
<td>Burst Length</td>
<td>2,4,8</td>
<td>2,4</td>
<td>2,4</td>
</tr>
<tr>
<td>Write Latency</td>
<td>1 Clock</td>
<td>CASL - 1</td>
<td>CASL - 1</td>
</tr>
</tbody>
</table>

FCRAM/Network-DRAM looks like DDR+  
*Can share controller with DDR SDRAM*
FCRAM Continued

Multiplexed address

Supports burst length of 2, but . . .

Multiplexed address

CL = 4

Burst length of 4 is natural
RLDRAMx vs FCRAMx

- Both fighting for same market
- RLDRAMx: more SRAM-like
- RLDRAMx: more aggressive roadmap
- RLDRAMx: more “random bandwidth”
- But...
- FCRAMx: available from multiple vendors, Toshiba and Samsung (and low capacity parts from Fujitsu)
- FCRAMx: more consistant delivery wrt roadmap
- FCRAMx: more designs in market.
- Technical & nonTechnical considerations
DDR ESDRAM Part I

“Single Transistor SRAM”
300 MHz, 600 mbps data rate
Always - close page - policy
16 Banks Internally
Deassert - Hidden Refresh
Read or Write Latency of 4 or 6 cycles
Fixed Burst Length of 8 beats
DDR ESDRAM Part II

Next generation HP PA-RISC “Mako” processor
Use 4 chips to form 32 MB ECC protected L2 DRAM cache

Accesses to same banks cannot be fully pipelined
### DDR ESDRAM Part III

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<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>VSS</td>
<td>VDDQ</td>
<td>VSS</td>
<td>A</td>
<td>VSS</td>
<td>VREF</td>
<td>VSS</td>
<td>A</td>
<td>VSS</td>
<td>VDDQ</td>
<td>VSS</td>
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<tr>
<td>B</td>
<td>DQ</td>
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<td>DQ</td>
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<td>A</td>
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<td>VDDQ</td>
<td>VSS</td>
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<td>A</td>
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<td>DQ</td>
<td>VSS</td>
<td>BA</td>
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<td>BA</td>
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<td>NC</td>
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<tr>
<td>F</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>VDD</td>
<td>BA</td>
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<td>M1</td>
<td>NC</td>
<td>VSS</td>
<td>DQ</td>
<td>DQ</td>
<td>DQ</td>
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</tbody>
</table>

**“Clamshell” pinout**

- **PCB Board**
- **Top**
- **Bottom**

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**Notes:**
- DDR ESDRAM Part III
- "Clamshell" pinout
- PCB Board
- "Top" and "Bottom"
MobileRAM

Where can we save power?

Temperature compensated self refresh
Partial array refresh

Array segmentation

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Where can we save power?
# CellularRAM/MobileSDR

<table>
<thead>
<tr>
<th>Features</th>
<th>CellularRAM</th>
<th>Mobile SDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus type</td>
<td>Burst Nor Flash</td>
<td>SDRAM</td>
</tr>
<tr>
<td>Clock Freq</td>
<td>&lt; 100 MHz</td>
<td>66 ~ 133 MHz</td>
</tr>
<tr>
<td>Density</td>
<td>16~128 Mb</td>
<td>64~512 Mb</td>
</tr>
<tr>
<td>t_RAC</td>
<td>~40 ns*</td>
<td>~50 ns @ 66 MHz</td>
</tr>
<tr>
<td>pipeline support</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td># Banks</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>Burst Length</td>
<td>4,8,16,32</td>
<td>2,4,8,page</td>
</tr>
</tbody>
</table>

*Hidden self refresh. DRAM returns wait states in case of collision with refresh

**CellularRAM** - lowest power, best relative performance

**CellularRAM** - limited data rate, not scalable

**Mobile DDR** - Coming online
eDRAM

Available in pre-constructed Macros
May be available in varying widths (292 now, 1168 later)
Fast row cycle time (sub 10ns)
Fast access time (5 to 13 ns)
Targetted toward speed or density
Pushing to replace SRAM for cache (4X denser)

Bandwidth
Performance
Capacity/Density
Latency
Cost

Intel 0.13um silicon - “Northwood” ~ 140mm$^2$ ~ ASP $150$
AMD 0.13um silicon - Athlon ~ 100 mm$^2$ ~ ASP $80$
DRAM 0.13um silicon - various ~ 60 mm$^2$ ~ ASP $3$~$4$
BlueGene L

- 130nm bulk
- 4 MB L3 eDRAM
- 1024b wide port
- 1/4 of core freq.
- Offchip signal interconnects overlayed over eDRAM macro
- (More e⁻ per bit)
- eDRAM may be faster than SRAM!
- Definitely more tolerant of SEU

IBM BlueGene L processor
Die overlay courtesy of IBM
Summary

DRAM is DRAM

What kind of "performance" do you want?