ENEE 759H, Spring 2005

Memory Systems: Architecture and Performance Analysis

(Rambus) XDR Memory System

Credit where credit is due:
Slides contain original artwork (© Jacob, Wang 2005)
Row Cycle Time Trends

- Commodity DRAM Devices Row Cycle Trend: -7% per year
- DDR SDRAM
- High-Performance DRAM Devices
- RLDRAM / FCRAM
- XDR
DRAM Datarate Trends

Commodity DRAM Devices Datarate:
~Doubling Every 3 Years (log scale)

- SDRAM (min burst:1)
- DDR SDRAM (min burst:2)
- DDR2 SDRAM (min burst:4)
- XDR (min burst:16) 3.2 Gb/s (differential pair)

New Generations of DRAM Devices (time)
XDR:

Next Gen DRAM Rambus Signalling Tech

- DRSL: Differential Rambus Signaling Level
- ODR: Octal Data Rate
- FlexPhase: Per bit de-skewing by controller
- Sub row/column access
XDR Features

- 3.2 Gbps data rate
- Low Voltage Differential Signalling
- Per bit deskewing control eliminates path length matching necessity
- Implementable on commodity 4 layer PCB with standard design rules
- Connector specification - RSN? (for embedded systems)
- Burst-of-16
- Sub-column commands
- Up to 36 devices per channel
- Similar to D-RDRAM, but...
XDR Device Block Diagram:

- **Common Command Bus**: Connection for various control signals.
- **Register**: Storage element for data.
- **Decode**: Logic for decoding commands.
- **Bank Array**: Memory storage unit with specific dimensions.
- **Sense Amp Array**: Amplification and sense of stored data.
- **Dynamic Width Demux**: Mechanism for selecting data widths.
- **Vterm**: Voltage termination point.

Key Specifications:
- **800 Mbps**: Data transfer rate for certain operations.
- **400 MHz**: Clock frequency for specific logic sections.
- **200 MHz**: Clock frequency for sense amp array.
- **3.2 Gbps**: Data transfer rate for dynamic width demux.

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**Bank Array**:
- Dimensions: $16 \times 16 \times 2^6 \times 2^{12}$
- **Bank 0**
- **Bank 7**

**Sense Amp Array**:
- Dimensions: $16 \times 16 \times 2^6$
- **Array 0**
- **Array 7**

**Conventional Sense Amp/Bank struct.**
DRSL Signaling:

- Data bits are transported by differential, point to point low voltage signals. **Differential Rambus Signaling Levels**
Octal Data Rate:

- 3.2 Gbps Data Rate
- 400 MHz reference clock signal

Diagram of PLL with 3.2 Gbps Data Rate and Octal Data Rate.
System Topology:

- Low chip count, high bandwidth DRAM memory system

Diagram:

- DRAM chip 1
  - 12 bits, 800 Mbps
  - Bi-directional point-to-point data bus
- DRAM chip 0
  - 16 bits, 3.2 Gbps
- Shift registers for Flexphase operation
- Multi-drop unidirectional address and command bus
- Path length matched point-to-point

XDR Memory Controller Interface
XDR Channel Routing

- Address/Command Bus signals are path length matched (800 Mbps)
- Flexphase makes it unnecessary to path length match data signals (3.2 Gbps)
FlexPhase:

FlexPhase: Per bit deskewing circuit

PLLA

latch

FlexPhase

3.2 Gbps Data Rate

latch

FlexPhase

3.2 Gbps Data Rate

DRAM Controller

DRAM Chip
Flexphase Benefits

- Flexphase buffering to adjust for phase variance across several bit-depths
- Need to recalibrate often (compensate for temp drift)
- No need to send reference clock/strobe signals
- No need to carefully match path lengths (simplifies board design)
Delay Read in Long Channel

- Adjust the bitlane delay to match phase differentials
- Each device can act as x1 DRAM device.

** Require device support, optional in XDR spec.
Write Delay in Long Channel

- Adjust the bitlane delay to match phase differentials (data arrives “in-phase” w.r.t. write command)
- Longer Read-Write turnarounds in long channel
Dynamic Width Control I

- Sub Row (Page) Addressing
- Sub column Access
Sub Row Command

Width of row = width per device X No. of devices

- Send along half/quarter row addresses, activate only half/quarter of row.
- More sophistication = More die cost, but saves power.
Sub Column Command

- A “column” is (typically) the “smallest addressable unit of memory”.
- Oops... device allows sub column access.
- Send along “sub column address”.
- Burst of 16 maintained, but instead of 16 bits x 16 beats, 1, 2, 4 bits x 16 beats.
9, 18, or 36 devices provide ECC support

- Same device used in ECC/non-ECC configuration.
- Provide chipkill support in x1 device mode!
No Write Buffer

Column Cmd

Data Bus

t\text{CAS}
(CAS access delay)

t\text{WR}
(Write delay)

t\text{CWD}
(WRITE delay)

Large Bubble Without Write Buffer

Bank Array

16 \times 16 \times 2^6 \times 2^{12}

Bank 0

Bank 7

Column Addr

Sub Col Ctl

16 x 16

Row decode

Col decode

Dynamic Width Demux (WR)

1:16 Demux

Dynamic Width Demux (RD)

16 x 16

3.2 Gbps

Bank Array

16 x 16 \times 2^6

Array 0

Array 7

Dynamic Width Demux (WR)

1:16 Demux

3.2 Gbps

 Byte Mask

byte mask decode

Reg decode

Reg decode

Reg decode

Reg decode

200 MHz
In XDR Devices that support ERAW, to different bank sets.

Odd Bank Array
16 x 16 x 2^6 x 2^{12}
Bank 1

Sense Amp Array
Array 1
16 x 16 x 2^6
Array 7
16 x 16

Byte Mask
Dynamic Width Demux (WR)
16
1:16 Demux
16/tCycle 200 MHz
termination
3.2 Gbps

Even Bank Array
16 x 16 x 2^6 x 2^{12}
Bank 0

Sense Amp Array
Array 0
16 x 16
Array 6
16 x 16

Dynamic Width Demux (RD)
16/tCycle 3.2 Gbps
16
Differences of Philosophy

SDRAM - Variants

- Controller
- Complex Interconnect
- Inexpensive Interface
- Simple Logic
- DRAM Chips

D-RDRAM, now XDR

- Controller
- (Flexphase)
- Complex Logic
- More Simplified Interconnect!
- ~expensive Interface
- Complex Logic
- DRAM Chips

Complexity Moved to DRAM