



Course Syllabus

ENEE 759h: High-Speed Memory Systems, Spring 2003

Bruce Jacob & David Wang

1. Basic Information

Time & Place

Lecture: TuTh 12:30–1:45 pm, AVW-2120

Instructors

Bruce L. Jacob: AVW-1325, blj@eng.umd.edu

David T. Wang: AVW-1418, davewang@wam.umd.edu

Class Home Page

<http://www.ece.umd.edu/courses/enee759h/>

Class Email List

enee759h-0101-spr03@coursemail.umd.edu

Class Schedule

This is a weekly schedule of my hours, including class time and scheduled office hours, but also including other things that make me unavailable. It is subject to change.

	Mon	Tue	Wed	Thu	Fri
9-9:30					
9:30-10					
10-10:30	Committee Meeting	ENES 100 (JMP-1202)		ENES 100 (JMP-1202)	
10:30-11					
11-11:30					Discussion (JMP-1202)
11:30-12					
12-12:30					Research Meeting
12:30-1		ENEE 759h (AVW-2120)		ENEE 759h (AVW-2120)	Meetings with graduate research assistants
1-1:30					
1:30-2					
2-2:30			Committee Meeting		
2:30-3					
3-3:30					
3:30-4					
4-4:30					

2. Course Overview

This course introduces students to the issues involved in high-speed chip-level interfaces in the context of DRAM systems design. General topics include high-speed signaling mechanisms, signal integrity, synchronization mechanisms, meeting skew budgets, packaging, and power consumption. DRAM-specific topics include studies of modern high-performance DRAMs (SDRAM, DDR, Rambus, FCRAM, RLDRAM) and future designs (DDR II, GDDR III, Rambus Yellowstone). Students will work in groups on a research-oriented project that may involve simulation, modeling, and/or fabrication of prototype chips.

3. Course Prerequisite(s)

Ideally, a student will have taken ENEE646 or perhaps ENEE446. Students must have knowledge of digital logic design and computer organization. For example, you should understand digital design concepts such as multiplexers, gates, boolean algebra, finite-state machines, and flip-flops. You should understand fundamental computer organization: what the program counter is, what a register file is for, how busses are used, what happens in the hardware to effect instruction execution, etc. It would help if you also understand and are reasonably fluent in programming Verilog (or C or Perl, because Verilog is very C-like, as is Perl).

4. Course Material

There is no required text for the course. Instead, we will provide you with PDF copies of the lecture slides, as well as PDF copies of supplemental material.

We recommend several particularly good texts:

- Dally & Poulton: *Digital Systems Engineering* — this presents an excellent coverage of the issues involved in designing high-speed chips and interfaces.
- Johnson & Graham: *High-Speed Digital Design* — similar to Dally & Poulton, this is an excellent look at the issues in designing high-speed chips and interfaces. Its approach is more practice-oriented than theory-oriented.
- Keeth & Baker: *DRAM Circuit Design* — this is a detailed look at the types of circuits that are used in modern DRAM design (i.e., buffers, drivers, decoders, sense amplifiers, etc.).
- Prince: *High Performance Memories* — this is a thorough overview of the types of memories that are available in the SRAM, DRAM, and video RAM classes.

In addition, we will use datasheets, whitepapers, and research articles to supplement the lectures. Because it is often worthwhile to go to the horse's mouth for information, when discussing some high-performance designs, we will go to the original descriptions of those designs, written by the designers.

5. Class Project

During the latter half of the semester we will conduct a group-oriented research project that will form the bulk of your grade in this class. The goal of the project will be to explore some facet (or facets, depending on the number of people involved) of high-speed memory systems. We might fabricate test chips to explore ideas, we might simulate high-speed interfaces in HSPICE, we might build models in C, etc. The project will be very intensive; be prepared to work hard. The topics and depth of investigation involved will be such that several could easily use this as a

stepping stone to their MS or PhD theses—i.e., Dave and I will decide on the topic and scope of the project/s. Here are a few ideas that we have for this semester:

- System protocol, interface, and signaling for a wave pipelined memory system.
- Design of a multi-channel system (fabricated through MOSIS).
- Page based operations in DRAM memory system.
- Investigation of serial-link memory system using existing I/O system technology. (i.e., serial ATA, NGIO, JAZiO, etc.)

For the latter half of the semester, be prepared to work 5–10 hours per week on the project.

6. Tentative Lecture Schedule

Week of	Subject	Notes
Jan. 27	–	
Feb. 3	Introduction to DRAMs and DRAM systems	
Feb. 10	Bus interfaces, address mappings, circuits and architectures	
Feb. 17	System topologies (bus, point-to-point)	Discuss Project
Feb. 24	High-frequency signalling	Feb. 25: AVW-3258
Mar. 3	SDRAM, DDR SDRAM	
Mar. 10	Rambus Direct RDRAM, example chipsets	
Mar. 17	Near-term future technologies DDR2, FCRAM, RLDRAM, GDDR3)	Lab Demo: Mar. 20
Mar. 24	Spring Break	
Mar. 31	Wires, Signalling	
Apr. 7	Timing, Synchronization	
Apr. 14	Case study: Rambus Yellowstone	
Apr. 21	Process, packaging, power consumption, modules	
Apr. 28	Alternative & embedded technologies	Lab Demo: May 1
May 5	Future trends & perspectives	
May 12	Project Presentations	

7. Special Needs

If you have a documented disability that requires special needs, please see me as soon as possible, and certainly no later than the third week of classes.