Configurations and Considerations for DDR Memory

Bill Gervasi
Chairman, JEDEC Memory Parametrics
Agenda

• DDR Market Takes Off!
• DDR Configurations
• The JEDEC Standards Process
• DIMMs & SO-DIMMs
• Making the Most of DDR Technology
• Previews of Coming Attractions
A Look at the DDR Market
DDR Market Takes Off!

Servers
Workstations
PC Segment 2
PC Segment 1
PC Segment 0
Mobile
Graphics

PC133
PC133
PC133
PC133
PC100
PC133

1H00 2H00 1H01 2H01

DDR DDR DDR DDR

Rambus DDR
DDR Configurations
DDR Configurations

- TSOP-II
- SO-DIMM
- DIMM
- TQFP
DDR Naming Conventions

• Chips have adopted “DDR” naming
  – Describes data rate per pin in MHz
  – **DDR-266A** is the fastest bin: 266 MHz data rate at CL 2.0
  – **DDR-266B** is the bulk bin: 266 MHz data rate at CL 2.5
  – **DDR-200** is the catchall bin: 200 MHz data rate at any CL

• Modules retain the “PC” name
  – Describes data rate per module in MB/s
  – **PC-2100** is the fastest bin: 2.1 GB/s on a 64 bit bus
  – **PC-1600** is the catchall bin: 1.6 GB/s on a 64 bit bus

• Small Systems specs retain “SS” name
  – **SS-333** and **SS-400** for 333 & 400 MHz data rates per pin
DDR Configurations, Chips

66 pin TSOP-II
- Used for DDR-266 and DDR-200
- Inexpensive high volume plastic package
- Compatible pinout for X4, X8, X16
- 64Mb to 512Mb; 1Gb in development

100 pin TQFP
- Used for SS-333 and SS-400
- Inexpensive high volume plastic package
- X32 configuration
- 64Mb and 128Mb
DDR Configurations, Modules

**Desktop & Server**
- 184 pins, 5.25” long
- X64 or X72 (ECC)
- 64MB to 2GB

**Mobile & Small Form Factor**
- 200 pins, 2.7” long
- X64 or X72 (ECC)
- 32MB to 512MB
JEDEC Standards Process
The JEDEC Standards Process

- JEDEC is a non-profit standards organization
- Suppliers & users and even competitors
- Working together to expand the market
How standards get done

Any company presents a market need
Interested companies form a Task Group
“Design assumptions” from end users
TG members take assignments
TG reviews simulations, promotes results:
- Rev 0.1 = Straw man proposal
- Rev 0.2 = TG agreement on approach
- Rev 0.3 = Passes simulation
- Rev 0.5 = Passes in hardware tester
- Rev 1.0 = Passes in end user hardware
Task Group to Committee

Task Group regularly reports to Committee
Ballot presented to Committee for vote
Votes addressed & suggestions gathered
Reballoted to achieve consensus
JEDEC publishes the results
  – Full reference design specification
  – Application notes from design assumptions
  – Free module gerbers for industry use
TG reforms as needed for ECOs, upgrades
Standards Process in Action: The DDR SO-DIMM
DDR SO-DIMM Standardization

• Initial concept by Hitachi and Transmeta
• Task Group formed:
  ALi, AMD, AMI2, AMP, ATP, Celestica, Hitachi, Hyundai, IBM,
  InterWorks, Kentron, Melco, Micron, Molex, PNY, Samsung,
  SiQual, Toshiba, Transmeta, Via
• Tasks divided:
  – AMP: socket definition
  – Hitachi: x16 chips, two bank
  – Samsung: x8 chips, one bank
  – Melco: x16 chips, one bank; x64 or x72 bus
DDR SO-DIMM Sockets

User Configuration

Height

Layout

End User Access
DDR SO-DIMM Assumptions

Flexible model accounts for real system layouts

<table>
<thead>
<tr>
<th>System</th>
<th>$L_{CRS}$</th>
<th>$L_{RSD0}$</th>
<th>$L_{D0D1}$</th>
<th>$L_{D1RT}$</th>
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</thead>
<tbody>
<tr>
<td>Base Assumption</td>
<td>60-90mm</td>
<td>10-15mm</td>
<td>10-15mm</td>
<td>10-15mm</td>
</tr>
</tbody>
</table>
DDR SO-DIMM Assumptions

Full system model developed for each signal
DDR SO-DIMM Simulations
Experimentation with layouts, termination
DDR SO-DIMM Status

• Task Group specification split into 4 sections
• ¾ of ballots submitted, all passed in June
• 4th section under vote now

Final approval expected in September
Standards Results:
The JEDEC Modules
DDR Unbuffered DIMM

- Least expensive module
- Limits number of loads supportable
- Address bus hits all DDR SDRAMs
- Fastest access time
DDR Registered DIMM

- Doubles density of each module or halves number of address buses needed
- Address bus latched before going to DDR SDRAMs
- Access time increased by one clock
When Size Matters

DIMM

50% smaller

SO-DIMM
DDR SO-DIMM

- Newest member of the DDR family
- Four configurations, support 32MB to 512MB

<table>
<thead>
<tr>
<th>Raw Card</th>
<th># DRAMs</th>
<th>Chip Org</th>
<th>Bus Width</th>
<th># Banks</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>8</td>
<td>X16</td>
<td>64</td>
<td>2</td>
<td>Highest density</td>
</tr>
<tr>
<td>B</td>
<td>8</td>
<td>X8</td>
<td>64</td>
<td>1</td>
<td>Highest density</td>
</tr>
<tr>
<td>C</td>
<td>4</td>
<td>X16</td>
<td>64</td>
<td>1</td>
<td>Lowest density</td>
</tr>
<tr>
<td>C</td>
<td>5</td>
<td>X16</td>
<td>72</td>
<td>1</td>
<td>ECC support</td>
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</tbody>
</table>
Butterfly SO-DIMMs

- Perfect for notebook, especially thin & light!
- Single access door to both SO-DIMMs
- Also good for small form factor desktop PCs
Making the Most of DDR Technology
Serial Presence Detect (SPD)

- Every DDR module contains an EEPROM
- Contains parameters for the module
  - Speed and access time
  - Number and organization of chips
  - Special features such as fast random access
  - Programmed by module supplier
- Systems use SPD to configure at boot time
- Without SPD, systems must use the most conservative timings!
## Power Management

<table>
<thead>
<tr>
<th>Power State*</th>
<th>Relative Power</th>
<th>Clocks of Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active on</td>
<td>100%</td>
<td>0</td>
</tr>
<tr>
<td>Inactive on</td>
<td>12%</td>
<td>3</td>
</tr>
<tr>
<td>Active off</td>
<td>4%</td>
<td>1</td>
</tr>
<tr>
<td>Inactive off</td>
<td>0.2%</td>
<td>4</td>
</tr>
<tr>
<td>Sleep</td>
<td>0.4%</td>
<td>200</td>
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</tbody>
</table>

* Not industry standard terms – simplified for brevity
Using Power States

- Power (mW)
- Active On
- Bank Access
- Task Demand Ramp
- Sleep
- Inactive Off
Power: DDR vs SDR

Throughput per Second per Unit Power

- PC-100 (1X)
- PC-133 (0.8X)
- DDR-266 (3X)
Previews of Coming Attractions
Next: Small Packages

FBGA
- Smaller footprint
- Lower inductance
- Tighter layouts enabled
Next: DDR FET Switched DIMM

- Quadruples density of each module or doubles number of DIMM slots
- Address bus latched before going to DDR SDRAMs
- Data bus sees a single load per slot
Next: DDR II

- Work well under way on DDR II
- Double the speed
- Lower power
- Migration path from DDR I
  - Same controller can use DDR I and DDR II
  - Compatible process technologies
Summary
Summary

• DDR explosion has begun
• Configurations for every application
  – TSOPs and TQFPs for point to point
  – Unbuffered & Registered DIMMs for desktops & servers
  – SO-DIMMs for mobile & small desktop
• JEDEC is the industry working together
DDR

Memory of choice for the future