This article reviews the chipkill correct memory architecture that is currently implemented in Dell™ PowerEdge™ 6400 and 6450 servers¹ and planned for future enterprise-class servers. This architecture is designed to improve reliability, availability, and serviceability (RAS), key requirements in enterprise-class servers used for mission-critical applications. The chipkill correct memory architecture allows the system to survive an important class of memory errors that would normally be fatal, thus helping to preserve customer data and maintain system availability.

**ECC Memory**

Standard error-correcting code (ECC) dynamic random-access memory (DRAM) systems provide for automatic correction when a single data bit is in error and for guaranteed detection of two data bits in error. This capability is often referred to as Single Error Correction/Double Error Detection (SEC/DED). However, when more than two data bits are in error on the same access, the errors may not be detected by a SEC/DED-based system, resulting in a data integrity failure. All detected multibit errors in this type of memory architecture are fatal and result in system downtime, while single-bit errors are automatically corrected in a manner that is transparent to the operating system and application programs.

ECC memory requires that some bits be dedicated to actual data and other bits to the ECC. DRAM devices are available in various data widths (number of data bits per device). The 168- and 184-pin dual in-line memory modules (DIMMs) used in servers today are built using x4 (4 data bit), x8, or x16 DRAM devices. The higher data bit DRAM devices are required to supply 72 bits of information (64 data bits and 8 ECC bits), because there is not enough physical space on the DIMM to use lower data-bit DRAMs.

**Memory Errors**

Memory errors are characterized as hard or soft. Hard errors are caused by defects in the silicon or metalization of the DRAM package, and are usually permanent once they manifest. Soft errors are caused by charged particles or radiation, and are transient. In the past, soft errors were primarily caused by alpha particles, but that failure mode has been mostly eliminated today by strict quality control of the packaging material by DRAM vendors. Currently the primary source of soft errors in DRAM is electrical disturbance caused by cosmic rays, which are very high-energy subatomic particles originating in outer space.

Many types of errors that occur in DRAM devices only impact one data bit, regardless of the width of the device. However, some error modes will result in more than one data bit being in error, up to the entire data width of the device. Any of these multibit failure modes result in a fatal error for a SEC/DED memory system, because only a single bit can be corrected by standard ECC. As DRAM devices become more dense, the percentage of errors that result in multibit failure increases. Furthermore, as server systems are built with larger memory capacities (using more and denser devices), the probability of either a soft or hard DRAM failure resulting in an uncorrectable error increases. Thus, the standard SEC/DED memory systems that provided very reliable operation a few years ago are becoming insufficient for the high RAS requirements of today’s servers.

This is particularly true for enterprise servers, which have memory requirements that are already over 4 gigabytes (GB). These requirements are expected to increase rapidly with the release of 64-bit processing systems. Studies indicate that the fatal error rate due to multibit memory errors within a single DRAM device in a server with 1 GB of system memory is about the same as a 32-megabyte (MB) server of several years ago that

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¹ The chipkill correct architecture is implemented in PowerEdge 6400 and 6450 servers that are equipped with 128-, 256-, and 512-MB DIMMs. Servers equipped with 64-MB DIMMs do not support the chipkill correct architecture.
only had parity memory support. The same reliability concerns that drove ECC for single-bit correction into enterprise servers several years ago (replacing parity) require the support of chipkill correction in these servers today.

**Chipkill Correct**

Chipkill correct is the ability of the memory system to withstand a multibit failure within a DRAM device, including a failure that causes incorrect data on all data bits of the device. There are two primary methods that can be used to provide chipkill correct memory, and combinations of these methods are also possible. These methods rely on the chip set and hardware architecture of the system and cannot be achieved through software upgrades.

In the first method, each data bit of a memory device is included in a separate “ECC word.” (An ECC word is the set of data bits and check bits over which the ECC algorithm provides for error detection and correction.) For example, a memory system can be designed to be 32 bytes (or 256 bits) wide. ECC bits are added so that the actual width of the memory data, plus ECC, is 288 bits. Four ECC words consisting of 64 data bits and 8 ECC bits each provide SEC/DED capability. These four ECC words are scattered, meaning that when using DIMMs that consist of x4 DRAM devices, the four bits of every device are scattered into separate ECC words. If a failure occurs that causes all four bits of the device to be in error, it results in single-bit errors within each ECC word and each is automatically corrected. In this example the memory system has chipkill correct only when DIMMs consisting of x4 DRAM devices are used. Figure 1 shows how this

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method works. Dell currently uses this method in its PowerEdge 6400 and 6450 servers.

A second method is to provide more ECC bits so that each ECC word can correct more than a single-bit failure. This is possible because there are different mathematical algorithms available that provide multiple-bit correction with the right number of data bits and ECC bits. For example, a 144-bit ECC word that consists of 128 data bits and 16 ECC bits can be used to correct up to 4 bit errors within certain bit fields of data. (These 4 bits must be adjacent, not random.) Even though the ratio of the ECC bits to data bits is the same as the previous example (16/128 vs. 8/64), the longer ECC word allows for a correction and detection algorithm that is more efficient.

A combination of these two methods can provide for chipkill correct support when using x8 DRAM devices. Two 144-bit ECC words can be scattered such that for each x8 DRAM device 4 bits are correctable in one ECC word and 4 bits are correctable in the second word. A memory system using this method provides chipkill correct when using DIMMs consisting of either x4 or x8 DRAM devices.

**Detection and Reporting**

Because the essence of chipkill support is a corrected memory failure, the detection and reporting mechanisms are identical to that of single-bit memory errors. There is no hardware or software performance penalty for the detection and reporting of chipkill events beyond what is standard today in ECC memory systems. Following is an overview of how hard or soft single-bit or chipkill events are detected and reported in Dell server designs.

The actual detection and correction of memory errors occurs within the system chip set silicon. ECC generation during write cycles and checking during read cycles occurs during every system memory transaction and is transparent to all application program software. If a correctable error is discovered, the data is automatically corrected before it is sent to the requesting agent. When this occurs, the event is recorded by the hardware, and the system BIOS (or the system abstraction layer [SAL] firmware used in the Intel® IA-64 architecture) is notified of the corrected error and where it occurred. The chip set also keeps a count of corrected errors so that the BIOS can determine if a hard error exists within a DIMM that is generating multiple corrected errors.

When notified, the system BIOS interrogates the registers in the chip set to determine where the memory error occurred. This determination is highly dependent on the design of a particular system, which is why it is handled at the BIOS level. When the BIOS identifies the DIMM that generated the error, it logs this information in the system event log that is a part of Dell’s Embedded Server Management architecture. Because the DIMM is a field-replaceable unit that may require predictive failure reporting and possible replacement, there is no need to resolve the error to a particular device within that DIMM. If the BIOS detects multiple corrected errors from the same DIMM in a short time period, it disables this error-reporting mechanism and logs this fact to the Embedded Server Management. This relieves the system of the processing overhead that takes place each time the BIOS is notified of a corrected memory error; a hard failure of a DRAM device could result in millions of corrected errors each minute. The hard error in the device is logged and the reporting mechanism is disabled to preserve the system’s performance.

The systems management instrumentation that is included with many Dell servers parses the system event log whenever the BIOS makes an entry. Events such as single-bit errors trigger one of three notification levels: “warning,” “critical,” and “nonrecoverable.” A true soft error that occurs once within a DRAM is not likely to trigger a notification to the systems management software stack. However, a degrading condition within a DIMM triggers notifications to the software so that service can be scheduled to replace the faulty DIMM. A hard failure that results in correctable error detection being disabled will always trigger a notification event. Although a hard single-bit or chipkill failure does not cause the system to go down, it does increase the risk that further soft failure events will cause a fatal, noncorrectable error. For this reason, system administrators must pay close attention to notifications of degraded DIMMs and schedule service to replace faulty devices.
Summary

Increasingly dense DRAM devices and very large memory support in enterprise servers requires a higher level of memory protection than standard (SEC/DED) ECC. Chipkill correction in Dell PowerEdge servers is designed to provide high reliability and availability required in server environments.

For More Information

The following paper is an excellent resource for more information on the research and analysis of memory DRAM failure modes and frequencies.


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