Executive Summary

- In 1992, Rambus introduced a new signaling technology, Rambus Signaling Level (RSL) at 500 MHz data rate to address high-bandwidth chip interconnect bottlenecks. RSL now supports 1066 MHz operation with plans for 1200 MHz.
- In 2000, Rambus introduced its next generation signaling technology, Quad Rambus Signaling Levels (QRSL™), offering twice the data rate per pin (>2 Gb/s/pin) of RSL.
- Also in 2000, Rambus introduced a new signaling technology called Quad Serializer/Deserializer (SerDes) which is a 3.125 Gb/s serial link for point-to-point applications.
- This paper discusses these three signaling technologies and their different market segments and application areas.

Signaling Technologies

Rambus offers three types of chip interconnection technology for bus and link topologies. The first is RSL which was introduced in 1992 and first productized in 1995 and is intended for multiple-connection busses, such as main-memory. Rambus’ newest signaling technology is called QRSL, and is intended for small, multiple-chip connection systems. These include small memory subsystems and chip-to-chip interconnects. The Quad SerDes interface, introduced earlier this year, is a high-speed serial point-to-point interface technology designed to connect two chips together across a backplane through connectors.

Rambus Signaling Level (RSL)

RSL was Rambus’ first signaling technology. Initially, RSL was introduced with data rate of 500 MHz and has since been enhanced over time to a 1066 MHz data rate.

RSL combines many techniques, topologies and circuits resulting in the ability for a system to run at these high data rates.

There are many key elements to RSL technology, such as:
- Low voltage swing (800 mV p-p)
- Current mode output drivers
- Automatic output current control
- Controlled impedance design, typically 28 to 40 Ohms, 30 mA maximum drive

![Figure 1: RSL Signal Levels](image1)

- Logic 0
  - $V_{term} \approx 1.8 \text{ V}$
- $0.8 \text{ V}$
- $V_{ref} \approx 1.4 \text{ V}$
- Logic 1
  - $V_{OL} \approx 1.0 \text{ V}$

![Figure 2: 1066 MHz RSL Eye Diagram](image2)
Quad Rambus Signaling Levels (QRSL)

QRSL is a new signaling technology, fundamentally different from RSL. Almost all chip interconnect technology today transfers data using binary information, representing 0’s and 1’s with two voltage levels. QRSL doubles the data rate by using four voltages to represent two bits of information. This multi-level signaling allows higher data bandwidth, twice that of RSL (>2Gb/s) while not increasing the frequency of operation of the Channel.

The following figure shows an eye diagram of a QRSL driver.

![QRSL Signal Levels](image)

**Figure 3: QRSL Signal Levels**

The major features of QRSL are:
- Low voltage swing (800 mV p-p, ~267 mV per step)
- Current mode output drivers
- Automatic output current control (for three drive levels)
- Controlled impedance design typically 40 Ohm systems
- Low parasitic packages
- Double data rate and multi-level signaling, providing four bits of information per clock cycle
- Gray coded logic levels
- Bi-directional Channel
- Pseudo-differential receivers, with three Vref inputs
- New driver and receiver circuits, including integrating receivers
- Common differential clock, which travels with the data, and is the same frequency as RSL
- Terminated at one end

Quad Serializer/Deserializer (SerDes)

In April 2000, Rambus disclosed a new signaling technology primarily intended for chip-to-chip and backplane interconnect. The first implementation runs at 3.125 Gb/s.

The following figure shows a SerDes eye diagram.

![SerDes Signal Levels](image)

**Figure 5: SerDes Signal Levels**

- Low voltage swing (500 mV differential) - programmable
- Current mode output drivers
- Output current set via external reference resistor
- Controlled impedance design, typically 50 Ohms differential, 20 mA drivers
- Data can be encoded with clock using 8b/10b encoding
- Unidirectional point-to-point interconnect topology, multiple bits in flight
- True differential signaling using two pins per driver and receiver
- Programmable internal termination via external reference resistor
- Transmitter and receiver clock sources need not be the same, but must be within tight frequency tolerance
- Designed to work across a long backplane (~30 in.) and through two connectors
Comparison of RSL, QRSL and SerDes

QRSL uses the same frequency clock as RSL, but transfers twice as may bits per clock edge by further subdividing the voltage swing into four levels. Figure 6 shows the same bit pattern being transmitted in RSL and twice in QRSL.

RSL and QRSL are for multi-drop busses and the SerDes technology is for point-to-point links.

The following table lists the major differences between the three signaling technologies.

<table>
<thead>
<tr>
<th>Application Areas</th>
<th>RSL</th>
<th>QRSL</th>
<th>Quad SerDes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main-Memory</td>
<td>Small Memories, Chip-to-Chip</td>
<td>Chip-to-Chip across backplanes</td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>Multi-drop, Bidirectional Bus</td>
<td>Multi-drop, Bidirectional Bus</td>
<td>Point-to-Point, unidirectional link</td>
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<tr>
<td>Data Rate per link</td>
<td>1066 MHz</td>
<td>&gt;2 Gb/s</td>
<td>3.125 Gb/s(^a) (4 links)</td>
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<tr>
<td>Number of Devices</td>
<td>up to 32 slaves</td>
<td>up to 4 slaves</td>
<td>2 devices</td>
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<td>Length of Interconnect</td>
<td>~ 20 in.</td>
<td>~ 4 in.</td>
<td>~ 30 in.</td>
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<tr>
<td>Connectors</td>
<td>Yes</td>
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<td>Backplane connectors</td>
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<tr>
<td>Voltage Swing</td>
<td>800 mV</td>
<td>800 mV</td>
<td>±500 mV(^b) differential</td>
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<td>Voltage Levels</td>
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<td>2</td>
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<td>Clock Frequency</td>
<td>533 MHz</td>
<td>&gt;500 MHz</td>
<td>Embedded Clock</td>
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<tr>
<td>Separate Clocks</td>
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<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Future Signaling Roadmap

As RSL has evolved over time, and has increased in frequency, future enhancements to all three signaling technologies will continue to push bandwidth/pin higher.

Figure 6: RSL and QRSL Signaling

Table 1: Signaling Technology Differences

Figure 7: Rambus Signaling Bandwidth Increases