

Executive Summary

- In 1992, Rambus introduced a new signaling technology, Rambus Signaling Level (RSL) at 500 MHz data rate to address high-bandwidth chip interconnect bottlenecks. RSL now supports 1066 MHz operation with plans for 1200 MHz
- In 2000, Rambus introduced its next generation signaling technology, Quad Rambus Signaling Levels (QRSL[™]), offering twice the data rate per pin (>2 Gb/s/pin) of RSL.
- Also in 2000, Rambus introduced a new signaling technology called Quad Serializer/Deserializer (SerDes) which is a 3.125 Gb/s serial link for point-to-point applications.
- This paper discusses these three signaling technologies and their different market segments and application areas.

Signaling Technologies

Rambus offers three types of chip interconnection technology for bus and link topologies. The first is RSL which was introduced in 1992 and first productized in 1995 and is intended for multiple-connection busses, such as main-memory. Rambus' newest signaling technology is called QRSL, and is intended for small, multiple-chip connection systems. These include small memory subsystems and chip-to-chip interconnects. The Quad SerDes interface, introduced earlier this year, is a high-speed serial point-to-point interface technology designed to connect two chips together across a backplane through connectors.

Rambus Signaling Level (RSL)

RSL was Rambus' first signaling technology. Initially, RSL was introduced with data rate of 500 MHz and has since been enhanced over time to a 1066 MHz data rate.

RSL combines many techniques, topologies and circuits resulting in the ability for a system to run at these high data rates.

There are many key elements to RSL technology, such as:

- Low voltage swing (800 mV p-p)
- Current mode output drivers
- Automatic output current control
- Controlled impedance design, typically 28 to 40 Ohms, 30 mA maximum drive

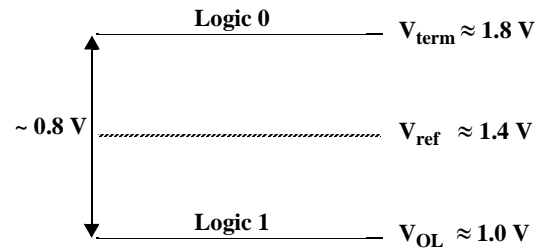


Figure 1: RSL Signal Levels

- Low parasitic packages
- Double data rate (transfers data on both edges of clock)
- Bi-directional bus, multiple data bits outstanding on the Channel at once
- Pseudo-differential signals, only one pin per signal with common Vref for all input samplers
- Uniform high-speed connection, not a mesh topology
- Advanced driver and receiver circuits on chip, including the use of DLLs
- Common differential clock travels with data and loops around in the controller
- Terminated at one end

The result of the combination of all these techniques is a signaling technology that transfers data at 1066 MHz with headroom to support higher frequencies in the future.

The following is an eye diagram of a RSL driver, showing high quality signaling.

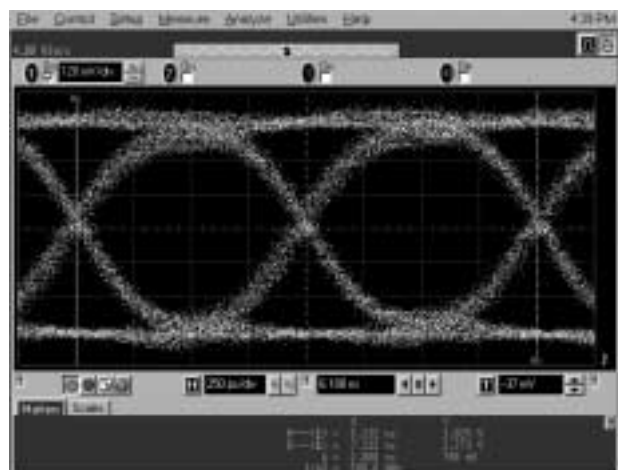


Figure 2: 1066 MHz RSL Eye Diagram



Quad Rambus Signaling Levels (QRSL)

QRSL is a new signaling technology, fundamentally different from RSL. Almost all chip interconnect technology today transfers data using binary information, representing 0's and 1's with two voltage levels. QRSL doubles the data rate by using four voltages to represent two bits of information. This multi-level signaling allows higher data bandwidth, twice that of RSL (>2Gb/s) while not increasing the frequency of operation of the Channel.

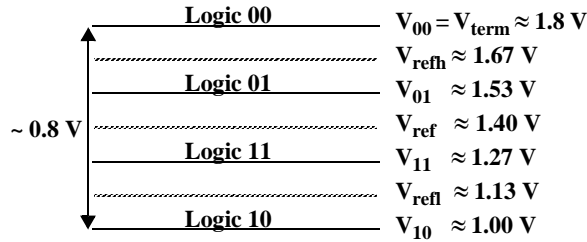


Figure 3: QRSL Signal Levels

The following figure shows an eye diagram of a QRSL driver.

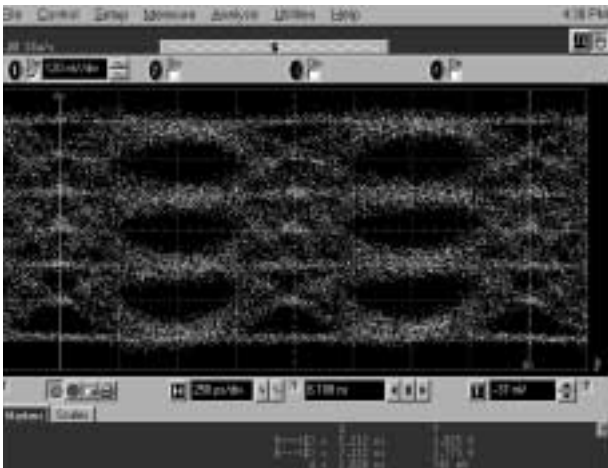


Figure 4: >2 Gb/s QRSL Eye Diagram

Major features of QRSL are:

- Low voltage swing (800 mV p-p, ~267 mV per step)
- Current mode output drivers
- Automatic output current control (for three drive levels)
- Controlled impedance design typically 40 Ohm systems
- Low parasitic packages

- Double data rate and multi-level signaling, providing four bits of information per clock cycle
- Gray coded logic levels
- Bi-directional Channel
- Pseudo-differential receivers, with three Vref inputs
- New driver and receiver circuits, including integrating receivers
- Common differential clock, which travels with the data, and is the same frequency as RSL
- Terminated at one end

Quad Serializer/Deserializer (SerDes)

In April 2000, Rambus disclosed a new signaling technology primarily intended for chip-to-chip and backplane interconnect. The first implementation runs at 3.125 Gb/s.

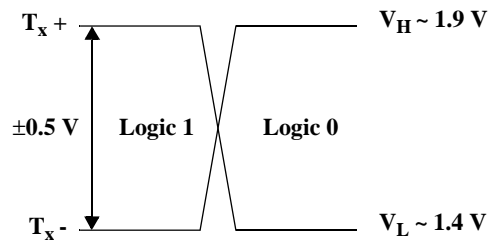


Figure 5: SerDes Signal Levels

- Low voltage swing (500 mV differential) - programmable
- Current mode output drivers
- Output current set via external reference resistor
- Controlled impedance design, typically 50 Ohms differential, 20 mA drivers
- Data can be encoded with clock using 8b/10b encoding
- Unidirectional point-to-point interconnect topology, multiple bits in flight
- True differential signaling using two pins per driver and receiver
- Programmable internal termination via external reference resistor
- Transmitter and receiver clock sources need not be the same, but must be within tight frequency tolerance
- Designed to work across a long backplane (~30 in.) and through two connectors



Comparison of RSL, QRSL and SerDes

QRSL uses the same frequency clock as RSL, but transfers twice as many bits per clock edge by further subdividing the voltage swing into four levels. Figure 6

shows the same bit pattern being transmitted in RSL and twice in QRSL.

RSL and QRSL are for multi-drop busses and the SerDes technology is for point-to-point links.

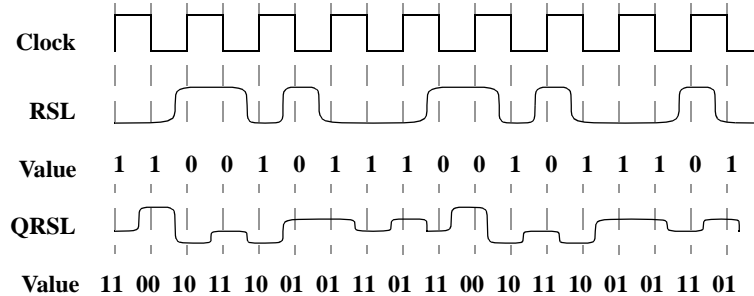


Figure 6: RSL and QRSL Signaling

The following table lists the major differences between the three signaling technologies.

Table 1: Signaling Technology Differences

	RSL	QRSL	Quad SerDes
Application Areas	Main-Memory	Small Memories, Chip-to-Chip	Chip-to-Chip across backplanes
Type	Multi-drop, Bidirectional Bus	Multi-drop, Bidirectional Bus	Point-to-Point, unidirectional link
Data Rate per link	1066 MHz	>2 Gb/s	3.125 Gb/s ^a (4 links)
Number of Devices	up to 32 slaves	up to 4 slaves	2 devices
Length of Interconnect	~ 20 in.	~ 4 in.	~ 30 in.
Connectors	Yes	Not initially	Backplane connectors
Voltage Swing	800 mV	800 mV	±500 mV differential ^b
Voltage Levels	2	4	2
Clock Frequency	533 MHz	>500 MHz	Embedded Clock
Separate Clocks	Yes	Yes	No

- a. SerDes uses a differential pair of pins per connection, and the data is encoded as 10 bits for every 8 bits transmitted, yielding 2.5 Gb/s per pair of pins.
- b. Two outputs switch at 500 mV each, yielding a 1V input differential input to the receiver, ignoring loss.

Future Signaling Roadmap

As RSL has evolved over time, and has increased in frequency, future enhancements to all three signaling technologies will continue to push bandwidth/pin higher.

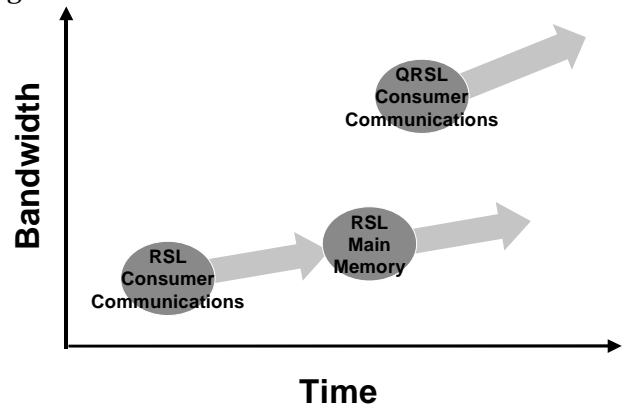


Figure 7: Rambus Signaling Bandwidth Increases



Copyright © June 2001, Rambus Inc. All rights reserved.

No part of this document may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means without the prior written permission of Rambus Inc.

Rambus, RDRAM, and the Rambus Logo are registered trademarks of Rambus Inc. Direct Rambus, Direct RDRAM, QRSL, RIMM, and SO-RIMM are trademarks of Rambus Inc.

Rambus Inc. assumes no responsibility or liability for any use of the information contained herein. Rambus components are manufactured and sold by Rambus partners. Rambus partners provide data sheets specific to their products. For a list of Rambus partners who are providing Rambus components, refer to the *Partner Pavilion* page on our website: <http://www.rambus.com>.

Data contained in this document is preliminary and subject to change without notice. Rambus Inc. assumes no responsibility for any errors that may appear in this document. Rambus Inc. makes no warranties, express or implied, of functionality or suitability for any purpose. No license is granted by its implication or otherwise under any patent or patent rights of Rambus Inc.

Rambus Inc.
4440 El Camino Real
Los Altos, California USA
94022

Telephone: (650) 947-5000
Fax (650) 947-5001