Rambus® 32 and 64 bit RIMM™ Module

Technology Summary

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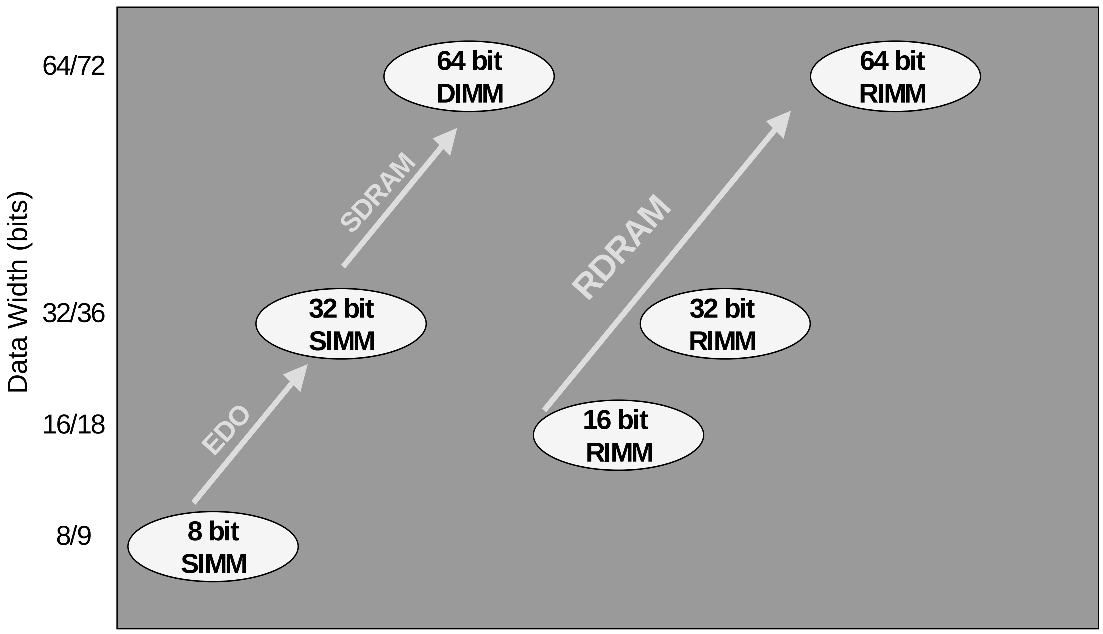
Introduction

Throughout the 15-year history of DRAM memory modules, two avenues have been used to increase the bandwidth supplied from a memory module: increased width and frequency. In the late 1980s, DRAMs were packaged on an 8 bit wide SIMM with up to eight components on a module. The evolution of DRAM modules led to 32 bit SIMMs that used page mode and EDO devices, followed by the more recent SDRAM DIMM with a data path width of 64 bits.

In 1999, Rambus® DRAM (RDRAM®) memory technology introduced an 8x increase over the pervasive PC100 in memory system operating frequency. This dramatic increase in data rate paved the way for the 16 bit wide RIMM. The 16 bit wide RIMM had the first-ever *decrease* in module and chipset interface data width while doubling the module bandwidth. Just as previous memory technologies used increased data width to allow increased module bandwidth, RIMM modules can provide a similar increase in width to provide increased module and system bandwidth without requiring major changes in DRAM devices or controllers connecting to them.

Figure 1: Module Data Width History



Technology Summary

In addition to the increased width, these RIMM modules will support a range of data frequencies. As shown in Table 1 all of RIMM modules support both 800 MHz and 1066 MHz operations. These operating frequencies are ideally suited for systems operating with base frequencies of 100 MHz and 133 MHz respectively. Table 1 also summarizes the features and technologies provided for various width modules.

Table 1: RIMM Technology Summary.

Module Type	16 bit RIMMs		32 bit RIMMs		64 bit RIMMs	
Module Name	RIMM1600	RIMM2100	RIMM3200	RIMM4200	RIMM6400	RIMM8500
RDRAM Data Frequency	800 MHz	1066 MHz	800 MHz	1066 MHz	800 MHz	1066 MHz
Module Data Width	16 or 18 bits	16 or 18 bits	32 or 36 bits	32 or 36 bits	64 or 72 bits	64 or 72 bits
Module BW in MB/s	1600	2133	3200	4266	6400	8532
Minimum Device Capacity	1	1	2	2	4	4
Maximum Device Capacity	16	16	16	16	16	16
Request busses	1	1	2	2	1	1
Shared Request Bus	No	No	No	No	Yes	Yes
Partial Data Termination	No	No	Yes	Yes	Yes	Yes
Byte masking suppport	Yes	Yes	Yes	Yes	No	No
ECC module width	18	18	36	36	72	72
Module pin count	168	168	232	232	326	326
Data bus impedance	28 Ohms	28 Ohms	40 Ohms	40 Ohms	40 Ohms	40 Ohms
Module Vdd	2.5 Volts	2.5 Volts	2.5 Volts	2.5 Volts	1.8 Volts	1.8 Volts
Module Vterm	none	none	1.8 Volts	1.8 Volts	1.5 -1.8 Volts	1.5 -1.8 Volts
Mesochronous Write Data	No	No	No	No	Yes	Yes

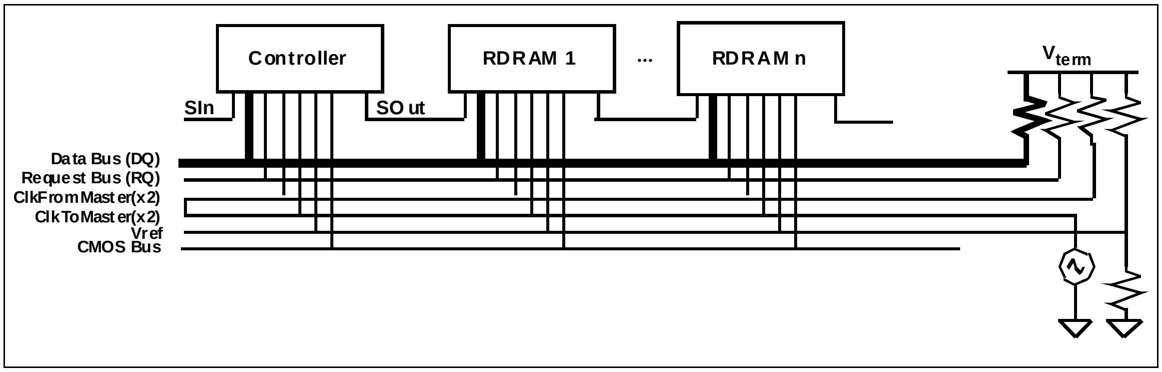
All RIMM modules use the conventional RDRAM and RSL signaling. In order to better understand the architecture of the 32 and 64 bit RIMM modules, a basic understanding of RDRAM and Rambus Signaling is necessary.

As shown in Figure 2, the interface to the RDRAM device is basically composed of two high speed buses: the request bus (RQ) and the data bus (DQ). A slower CMOS bus is used for initialization and power management. For a more detailed description of the operation of the RDRAM device, refer to the RDRAM datasheet.

The request bus is an 8 bit bus used to communicate control and address information from the controller to the RDRAM device and is sampled synchronously by the RDRAM device with the ClockFromMaster differential clock pair. The data bus is a 16 bit wide bus (18 for ECC systems) that carries data to and from the RDRAM device for writes and reads respectively. The data bus is sometimes referred to as being two bytes wide, with one byte called the “A byte” and the second, the “B byte”. Write data travels from the controller to the RDRAM device across the data bus and sampled synchronously with the ClockFromMaster differential clock pair. Read data is transmitted from the RDRAM device to the controller on the data bus and transmitted by the RDRAM device synchronously, with the differential clock travelling in the same direction—ClockToMaster. This clock is then used at the controller for sampling the read data.

The request bus and the data bus are routed as transmission lines with the bus passing by the RDRAM devices before terminating at the end of the bus opposite the controller. The termination is achieved through a pull-up resistor to the termination voltage Vterm. This termination resistor is matched to the effective impedance of the bus after the effects of the device loading and routing are included.

Figure 2: RDRAM System Architecture

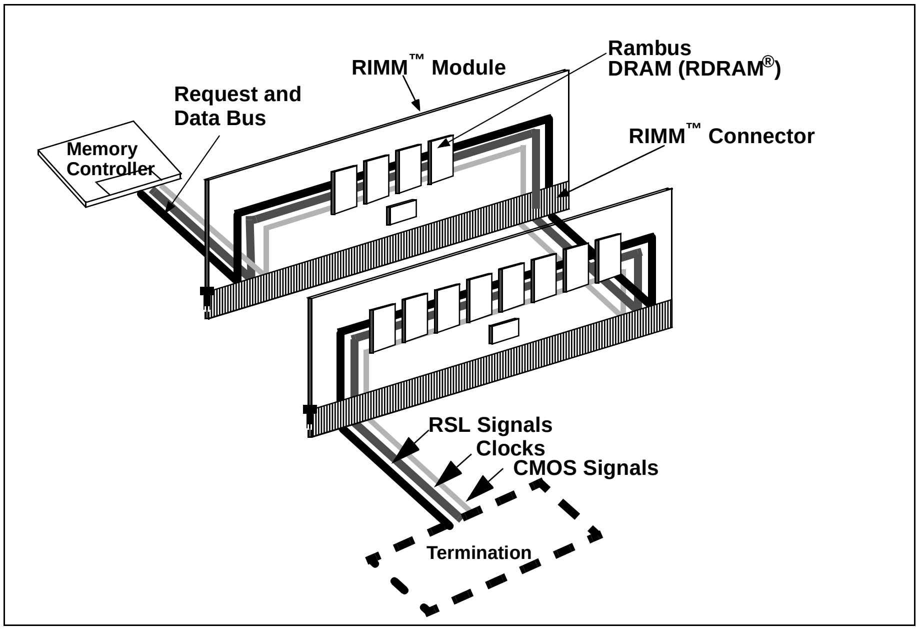


The CMOS bus is a slower speed bus used primarily for initialization. It comprises a serial chain of SIn and SOut sequencing in daisy chain between devices, A clock, SCK, and a command signal. The command signal, CMD, is routed as a bus to the device, signals commands and is used for timing generation..

16 bit RIMM Architecture

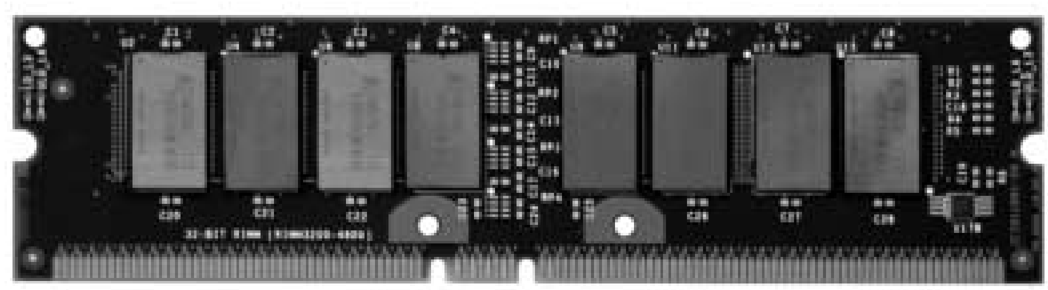
In a 16 bit RIMM system, the request and data bus are matched and routed through the RIMM module. All busses pass through the module, and continue on to a second (optional) module before being terminated on the motherboard after they exit the last module. *ClockFromMaster* is routed in the same way as the request and data bus and terminated after exiting the last module. ClockToMaster is typically sourced at the far end of the channel by the clock source and travels to the controller where it is looped back to become ClockFrom Master. In these systems, termination is provided on the motherboard and all signals are terminated together after passing through the modules.

Figure 3: 16 bit RIMM System



32 bit RIMM Features

Figure 4: 32 bit RIMM Module



Module-based Termination

A sample 32 bit RIMM module is shown in Figure 4. It is a 16 device module (eight additional devices are on the back of the module) capable of providing up to 4.2 GB/s of bandwidth. The center of the module contains termination resistors for the request and data bus of the terminated bus. Termination for the CMOS bus is located on the right-hand side of the module. In addtion to the termination, the module contains the SPD PROM used for storing information about the speed and capacity of the module and all necessary bypass capacitors. This module is routed on an eight layer board. Smaller density modules can be routed in six layers.

As mentioned earlier, RSL signals must be terminated, however, they do not need to be terminated in the same physical location. The 32 bit RIMM modules provide system-level termination through partial termination on the module. As shown in Figure 5, only half of the data bus is terminated on the module and the other half continues through the module. This half can be terminated on the motherboard in single module systems or continue through to the second module before being terminated there. One-half of the data bus terminated on the first module corresponds to the portion that is routed through the second module. On both the 32 and 64 bit RIMM modules, the CMOS bus is routed onto the module and terminated there.

Lower Vterm, and Higher Termination Resistance

Allowing reduced power and simpler interfacing to advanced silicon processing, the Vterm allows an operating range down to 1.5V. Additionally, the 64 bit RIMM module operates with impedance of 40 ohms, allowing narrower traces and lower power.

Support for Vterm reduction down to 1.5V.

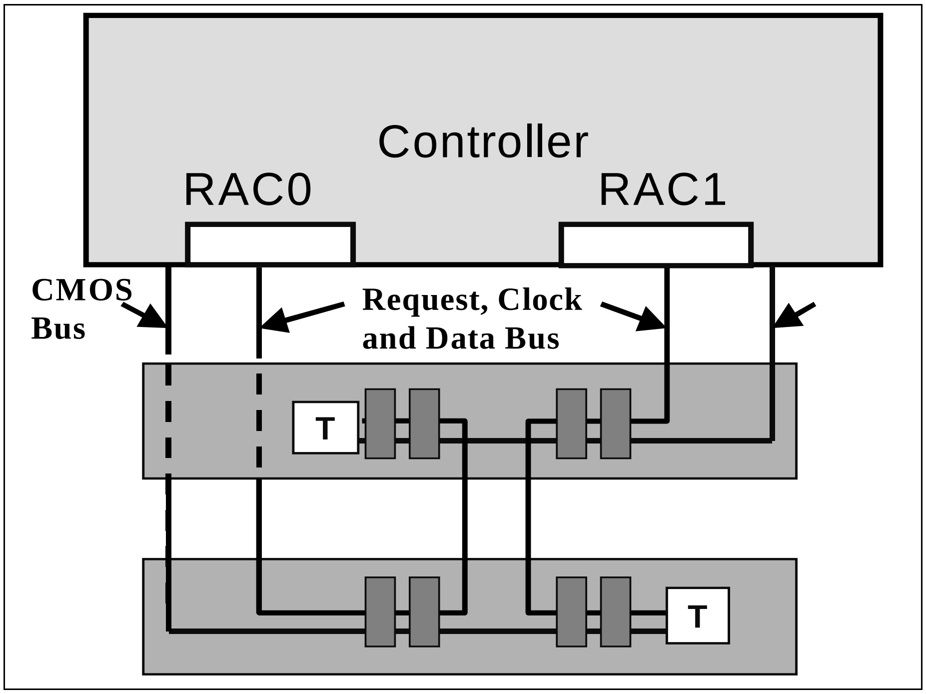
- 30% reduction in device I/O power

40-Ohm termination allows

- 30% reduction in termination power
- 30% reduction in device I/O Power

Reduced I/O current allowing better device performance

Figure 5: 32 bit RIMM System Configuration



64 bit RIMM Features

The Rambus 64 bit RIMM module is the next step in the evolution of the RDRAM memory roadmap. The 64 bit RIMM module achieves a greater than 4x increase in module bandwidth. This is accomplished primarily by increasing the data width to 64 bits—a departure from the 16 bit width of today's commodity RIMM modules.

The 64 bit RIMM module fufills many of the future high-bandwidth memory system needs.

- Lowest system cost for high bandwidth controllers and CPUs
- Full bandwidth necessary for future memory systems from a single module
- Controllers that support both the 64, 16 or 32 bit RIMM modules
- Simpler package escape routing, less restrictive signal matching, and four-layer motherboards
- 8.5 GB/s of bandwidth in a cost-effective memory configuration of only four DRAMs
- Improved voltage interface compatible with future advanced silicon processing
- Reduced Vdd for lower power and longevity
- Error correction support using a 72-bit option
- 128 MB to 2 GB module capacity support

Figure 6: 64 bit RIMM Module Topology

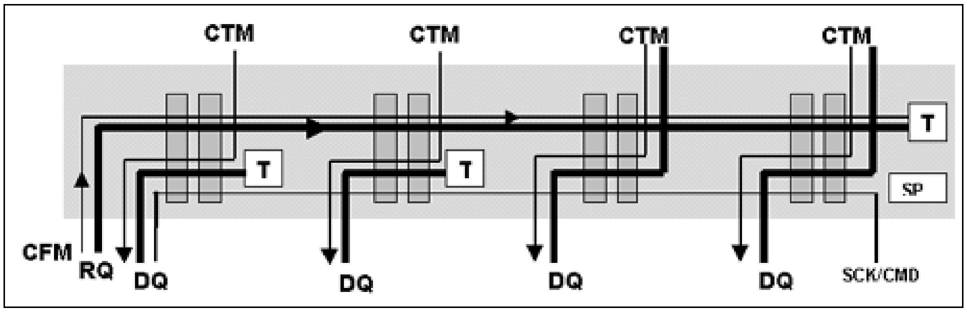


Table 2: 64 bit RIMM Module Pin Summary

Signal	Pins
RQ	8
DQ	108
CTM/CTMN	12
CFM/CFMN	2
SCK/CMD	2
SIO	2
SPD	8
NC	0
Vref	2
Vterm	16
Vcmos	4
Vdd	12
Other/Gnd	150
TOTAL	**326**

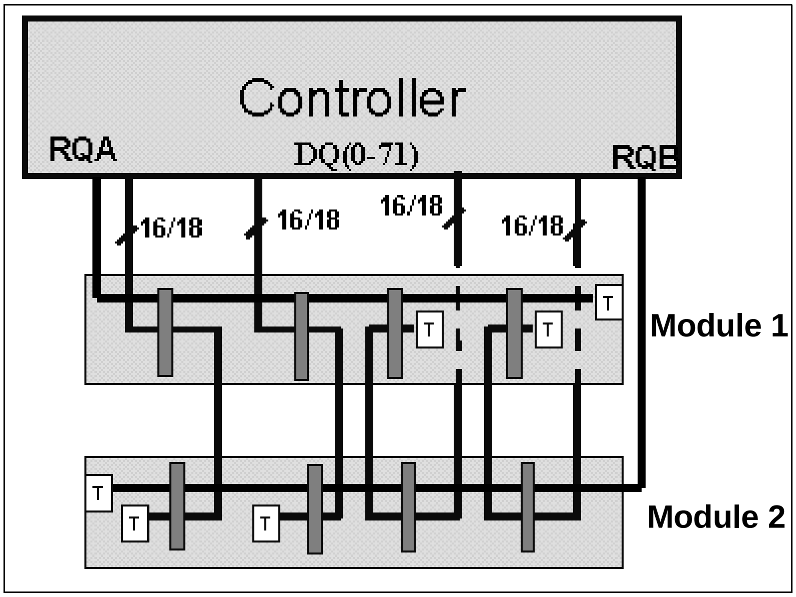
Shared Request

In a 16 bit and 32 bit RIMM module, the data and address are routed together and must be matched in length and loading. The Rambus 64 bit RIMM module allows a single request bus with a single differential transmit clock to provide address and control information to the entire module. This feature simplifies motherboard routing and saves pins on the module and controller. The shared address bus does not need to be matched to the data buses.

On-module Termination

A Rambus Channel includes high-speed, controlled-impedance matched transmission lines that must be terminated at the end furthest from the controller. The 64 bit RIMM module provides system-level termination through partial termination on the module. As shown in Figure 7, the request bus is terminated entirely on the module. However, only half of the data bus is terminated on the module and the other half continues through the module. This half can be terminated on the motherboard in single module systems or continue through to the second module before being terminated. The data bus half terminated on the first module corresponds to the portion routed through the second module.

Figure 7: System-level Configuration



Clocking

The Rambus Channel is synchronous, that is, all commands and data are referenced to clock edges. Special care must be taken to minimize clock-to-data skew at Rambus frequencies. At the physical level, data is transferred across the DQ lines only; all control information is sent across the ROW and COL pins. The RQ bus is source matched to the CFM clock on each module. All read data is synchronous with a clock CTM for each 16/18 bit data bus. However, write data must be aligned by the controller to arrive at the destination module, synchronous with the CFM clock. This unique clocking approach allows simpler motherboard routing because the data bus only needs to be matched to the CTM and the Request bus only needs to be matched to the CFM. No matching is required between the data buses or between data and request.

Vdd Reduction

The 64 bit RIMM module provides a Vdd of 1.8V, which is consistent with future DRAM process. The lower Vdd, reduces power, and eliminates the need for the 2.5V supply. The 64 bit RIMM module can be operated in thermal environments that are comparable to today's 16 bit RIMM modules, but without the need for additional cooling assistance.

Lower Vterm, and Higher Termination Resistance

By allowing reduced power and simpler interfacing to advanced silicon processing, the Vterm allows an operating range down to 1.5V. Additionally, the 64 bit RIMM module operates with an impedance of 40 ohms that allows narrower traces and lower power.

Support for Vterm reduction down to 1.5V.

- 30% reduction in device I/O power

40-Ohm termination allows

- 30% reduction in termination power
- 30% reduction in device I/O power
- Reduced I/O current allowing for better device performance

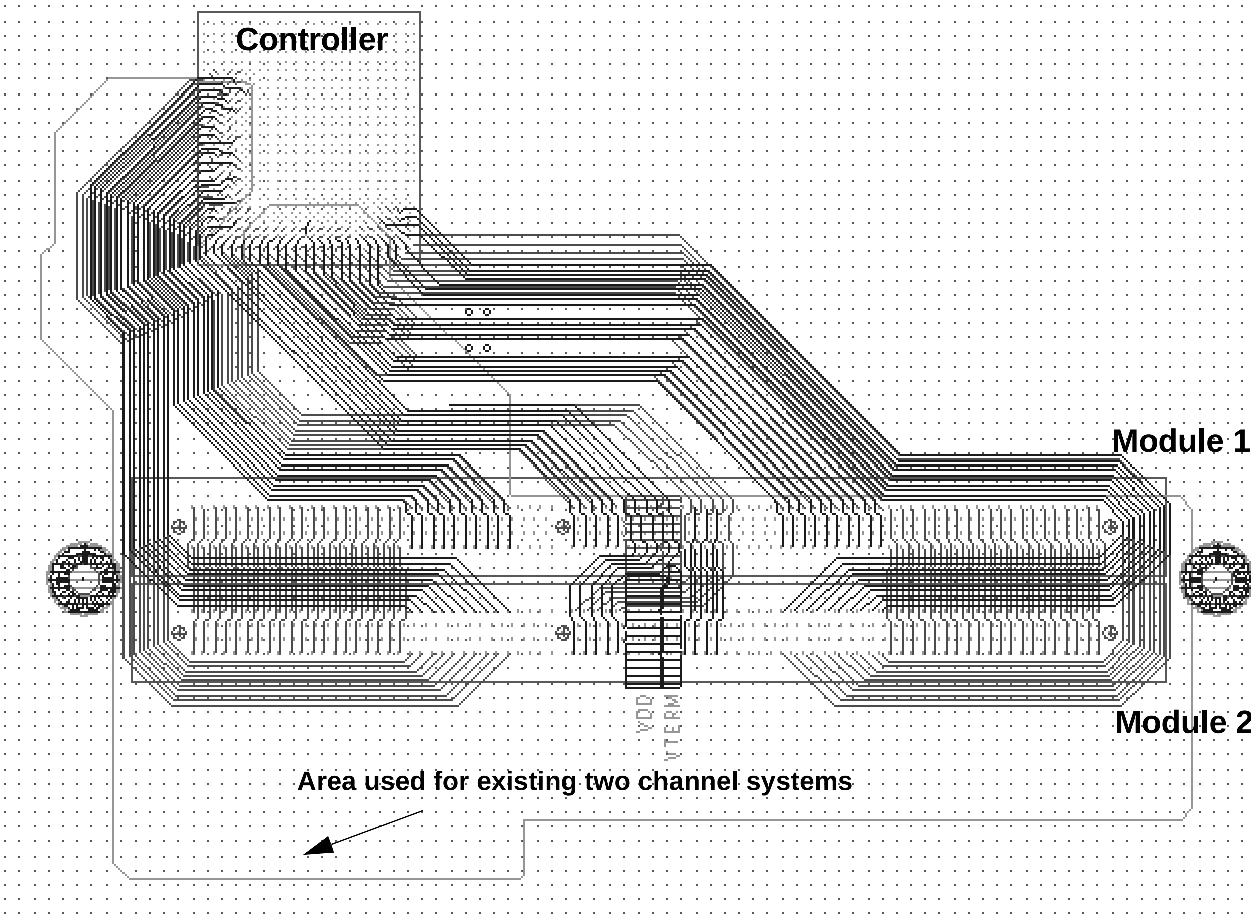
System Routing

Figure 8 illustrates the escape routing and channel routing for a two-module Rambus 64 bit RIMM module system. The higher impedance channel routing allows the 64/72 bit data path to be routed in less PCB area than existing two-channel systems.

Features of the sample routing include:

- 4-layer PCB supported
- 72 DQ bits and 2 RQ buses
- 10 mil trace escapes from 4 row deep
- Same ball grid array area as existing 2 RAC chipset

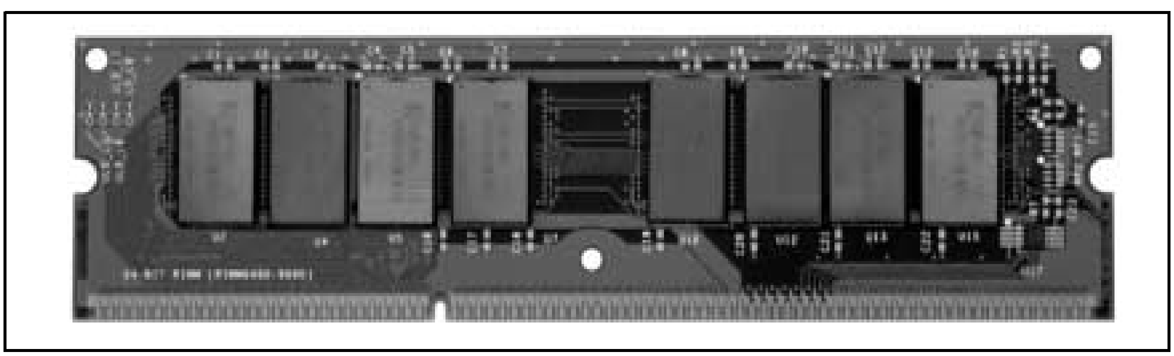
Figure 8: PCB Layout w/64 bit RIMM Modules



Module Routing

The 64 bit RIMM module can be routed in the same layer count and PCB size as existing 16 bit RIMM modules. For the 16 device (eight additional devices are located on the back) module shown in Figure 9, eight layers of PCB are required, while lower density four and eight device modules require only six layers.

Figure 9: 64 bit RIMM Module

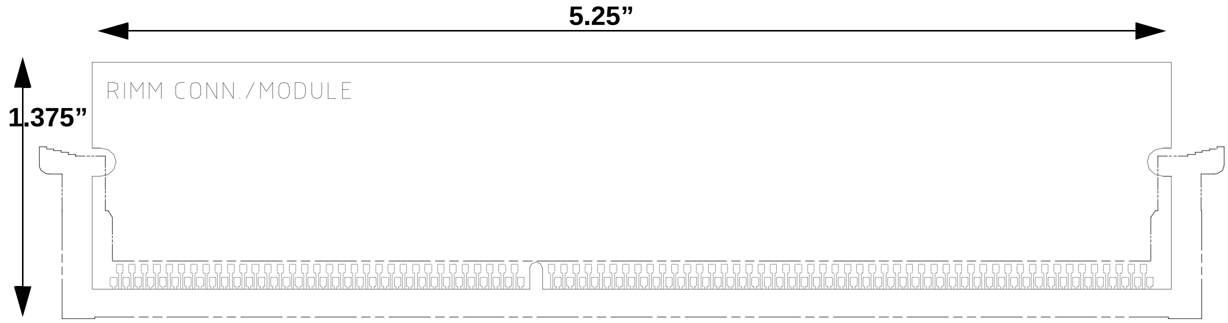


Connector Technology

The Rambus 64 bit RIMM module uses a 326-pin connector at a pin pitch of 0.76 mm and two contact rows for high pin density. A chamfered module and the two contact rows keep insertion force to that comparable to existing 16 bit RIMM modules.

At 1.375" high and 5.25" in length, the module and connector fit within the space of today's 16 bit RIMMand DIMM modules and provides the same look and feel as conventional RIMM upgrades.

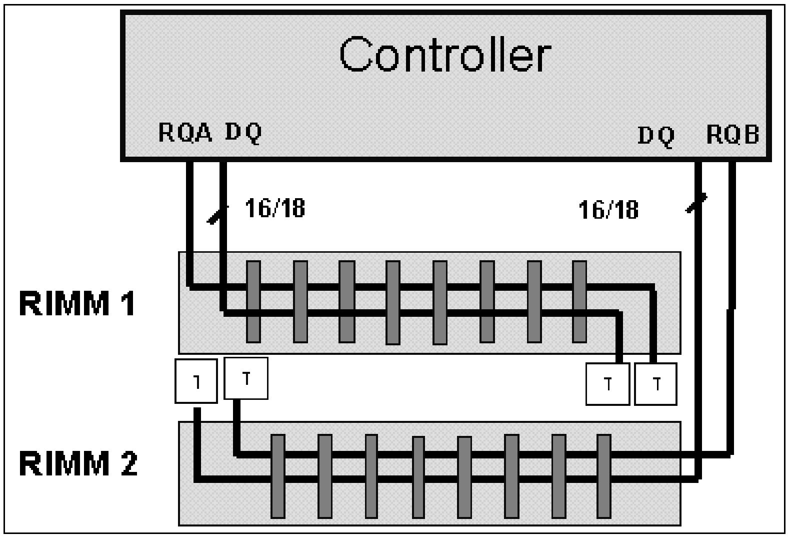
Figure 10: 326-pin Connector



Controller-compatible with 16 bit RIMM Modules

Controllers can be designed to support both the Rambus 64 bit RIMM and existing 16 bit RIMM modules. The controller shown in Figure 11 operates with conventional 16 bit RIMM modules enabling controllers to span the lower performance 16 bit RIMM module space through the 8.5 GB/s provided by the Rambus 64 bit RIMM module.

Figure 11: RIMM Support



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