512Mb/256Mb 1.8V NAND Flash Errata

Description: Some of AC characteristics are not meeting the specification.
> AC characteristics: Refer to Table

Affected Products: K9F1208Q0A-DCB0/DIB0, K9F1216Q0A-DCB0/DIB0
K9F5608Q0C-DCB0/DIB0, K9F5616Q0C-DCB0/DIB0
K9K1208Q0C-DCB0/DIB0, K9K1216Q0C-DCB0/DIB0

Improvement schedule: The components without this restriction will be available from work week 23 or after.

Workaround: Relax the relevant timing parameters according to the table.

Table

<table>
<thead>
<tr>
<th>Parameters</th>
<th>tWC</th>
<th>tWH</th>
<th>tWP</th>
<th>tRC</th>
<th>tREH</th>
<th>tRP</th>
<th>tREA</th>
<th>tCEA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>45</td>
<td>15</td>
<td>25</td>
<td>50</td>
<td>15</td>
<td>25</td>
<td>30</td>
<td>45</td>
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<tr>
<td>Relaxed Condition</td>
<td>60</td>
<td>20</td>
<td>40</td>
<td>60</td>
<td>20</td>
<td>40</td>
<td>40</td>
<td>55</td>
</tr>
</tbody>
</table>

UNIT: ns

Sincerely,
chwoosun@sec.samsung.com

Product Planning & Application Eng.
Memory Division
Samsung Electronics Co.
**Document Title**

64M x 8 Bit, 32M x 16 Bit NAND Flash Memory

**Revision History**

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>History</th>
<th>Draft Date</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>Initial issue.</td>
<td>Apr. 25th 2002</td>
<td>Preliminary</td>
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<tr>
<td>0.1</td>
<td>TBGA(K9F12XXX0A-DCB0/DIB0) size information is changed. (before) 9 x 11 /0.8mm pitch , Width 1.0 mm (after) To Be Decided.</td>
<td>May 9th 2002</td>
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<td>0.2</td>
<td>TBGA(K9F12XXX0A-DCB0/DIB0) size information is changed. (before) 9 x 11 /0.8mm pitch , Width 1.0 mm, to (after) 8.5 x 15 /0.8mm pitch, Width 1.0mm</td>
<td>July 10th 2002</td>
<td></td>
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<tr>
<td>0.3</td>
<td>Pin numbering includes TBGA Dummy ball. (Page5)</td>
<td>Aug 10th 2002</td>
<td></td>
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<tr>
<td>0.4</td>
<td>Pin numbering excludes TBGA Dummy ball. (Page5) Pin assignment of TBGA dummy ball is changed. (before) DNU --&gt; (after) N.C</td>
<td>Oct 21th 2002</td>
<td></td>
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<tr>
<td>0.5</td>
<td>1. Add the Rp vs tr,tf &amp; Rp vs ibusy graph for 1.8V device (Page 43) 2. Add the data protection Vcc guidence for 1.8V device - below about 1.1V. (Page 44)</td>
<td>Nov 21th 2002</td>
<td></td>
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<tr>
<td>0.6</td>
<td>The min. Vcc value 1.8V devices is changed. K9F12XXQ0A : Vcc 1.65V<del>1.95V --&gt; 1.70V</del>1.95V</td>
<td>Mar 5th 2003</td>
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<tr>
<td>0.7</td>
<td>Pb-free Package is added. K9F1208U0A-FCB0,FIB0 K9F1208Q0A-HCB0,HIB0 K9F1216U0A-HCB0,HIB0 K9F1216U0A-PCB0,PIB0 K9F1216Q0A-HCB0,HIB0 K9F1208U0A-HCB0,HIB0 K9F1208U0A-PCB0,PIB0</td>
<td>Mar 13rd 2003</td>
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<td>0.8</td>
<td>Errata is added.(Front Page)-K9F12XXQ0A</td>
<td>Mar 17th 2003</td>
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**Specification**

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<tr>
<th>tWC</th>
<th>tWP</th>
<th>tRC</th>
<th>tREH</th>
<th>tRP</th>
<th>tREA</th>
<th>tCEA</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
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<td>50</td>
<td>15</td>
<td>25</td>
<td>30</td>
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</tbody>
</table>

Note: For more detailed features and specifications including FAQ, please refer to Samsung’s Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

The attached datasheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions about device. If you have any questions, please contact the SAMSUNG branch office near you.
64M x 8 Bit / 32M x 16 Bit NAND Flash Memory

PRODUCT LIST

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Vcc Range</th>
<th>Organization</th>
<th>PKG Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>K9F1208Q0A-D,H</td>
<td>1.70 ~ 1.95V</td>
<td>X8</td>
<td>TBGA</td>
</tr>
<tr>
<td>K9F1216Q0A-D,H</td>
<td>2.7 ~ 3.6V</td>
<td>X16</td>
<td>TBGA</td>
</tr>
<tr>
<td>K9F1208U0A-Y,P</td>
<td></td>
<td>X8</td>
<td>TSOP1</td>
</tr>
<tr>
<td>K9F1208U0A-V,F</td>
<td></td>
<td>X8</td>
<td>WSOP1</td>
</tr>
<tr>
<td>K9F1216U0A-Y,P</td>
<td></td>
<td>X16</td>
<td>TSOP1</td>
</tr>
</tbody>
</table>

FEATURES

- Voltage Supply
  - 1.8V device(K9F12XXQ0A) : 1.70 ~ 1.95V
  - 3.3V device(K9F12XXU0A) : 2.7 ~ 3.6V
- Organization
  - Memory Cell Array
    - X8 device(K9F1208X0A) : (64M + 2048K) bit x 8 bit
    - X16 device(K9F1216X0A) : (32M + 1024K) bit x 16 bit
  - Data Register
    - X8 device(K9F1208X0A) : (512 + 16) bit
    - X16 device(K9F1216X0A) : (256 + 8) bit
- Automatic Program and Erase
  - Page Program
    - X8 device(K9F1208X0A) : (512 + 16) Byte
    - X16 device(K9F1216X0A) : (256 + 8) Word
  - Block Erase
    - X8 device(K9F1208X0A) : (16K + 512) Byte
    - X16 device(K9F1216X0A) : (8K + 256) Word
- Page Read Operation
  - Page Size
    - X8 device(K9F1208X0A) : (512 + 16) Byte
    - X16 device(K9F1216X0A) : (256 + 8) Word
  - Random Access : 12µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back
- Unique ID for Copyright Protection
- Package
  - K9F12XXU0A-YCB0/YIB0
  - 48 - Pin TSOP I (12x20 / 0.5 mm pitch)
  - K9F12XXU0A-DCH0/DIB0
  - 63- Ball TBGA
  - K9F1208U0A-VCB0/VIB0
  - 48 - Pin WSOP I (12X17X0.7mm)
  - K9F12XXU0A-PCB0/PIB0
  - 48 - Pin TSOP I (12x20 / 0.5 mm pitch)- Pb-free Package
  - K9F12XXU0A-HCB0/HIB0
  - 63- Ball TBGA - Pb-free Package
  - K9F1208U0A-FCB0/FIB0
  - 48 - Pin WSOP I (12X17X0.7mm)- Pb-free Package

GENERAL DESCRIPTION

Offered in 64Mx8bit or 32Mx16bit, the K9F12XX0A is 512M bit with spare 16M bit capacity. The device is offered in 1.8V or 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 200µs on the 528-byte(X8 device) or 264-word(X16 device) page and an erase operation can be performed in typical 2ms on a 16k-byte(X8 device) or 8k-word(X16 device) block. Data in the page can be read out at 50ns cycle time per word. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F12XX0A’s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The K9F12XX0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.
PIN CONFIGURATION (TBGA)

K9F12XXX0A-DCB0,HCB0/DIB0,HIB0

Top View
63-Ball TBGA (measured in millimeters)
PIN CONFIGURATION (WSOP1)

K9F1208U0A-VCB0,FCB0/VIB0,FIB0

PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F

Unit :mm
### PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
</table>
| I/O0 ~ I/O7 (K9F1208X0A) | DATA INPUTS/OUTPUTS  
The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. I/O8 ~ I/O15 are used only in X16 organization device. Since command input and address input are x8 operation, I/O8 ~ I/O15 are not used to input command & address. I/O8 ~ I/O15 are used only for data input and output. |
| CLE | COMMAND LATCH ENABLE  
The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal. |
| ALE | ADDRESS LATCH ENABLE  
The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of the WE with ALE high. |
| CE | CHIP ENABLE  
The CE input is the device selection control. When the device is in the Busy state, CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE control during read operation, refer to "Page read" section of Device operation. |
| RE | READ ENABLE  
The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one. |
| WE | WRITE ENABLE  
The WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse. |
| WP | WRITE PROTECT  
The WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low. |
| R/B | READY/BUSY OUTPUT  
The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. |
| VccQ | OUTPUT BUFFER POWER  
VccQ is the power supply for Output Buffer. VccQ is internally connected to Vcc, thus should be biased to Vcc. |
| Vcc | POWER  
Vcc is the power supply for device. |
| Vss | GROUND |
| N.C | NO CONNECTION  
Lead is not internally connected. |
| DNU | DO NOT USE  
Leave it disconnected. |

**NOTE**: Connect all Vcc and Vss pins of each device to common power supply outputs. Do not leave Vcc or Vss disconnected.
Figure 1-1. K9F1208X0A (X8) FUNCTIONAL BLOCK DIAGRAM

Figure 2-1. K9F1208X0A (X8) ARRAY ORGANIZATION

<table>
<thead>
<tr>
<th>Column Address</th>
<th>Row Address (Page Address)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O 0</td>
<td>1st Cycle</td>
</tr>
<tr>
<td>I/O 1</td>
<td>A0</td>
</tr>
<tr>
<td>I/O 2</td>
<td>A1</td>
</tr>
<tr>
<td>I/O 3</td>
<td>A2</td>
</tr>
<tr>
<td>I/O 4</td>
<td>A3</td>
</tr>
<tr>
<td>I/O 5</td>
<td>A4</td>
</tr>
<tr>
<td>I/O 6</td>
<td>A5</td>
</tr>
<tr>
<td>I/O 7</td>
<td>A6</td>
</tr>
<tr>
<td></td>
<td>A7</td>
</tr>
</tbody>
</table>

NOTE: Column Address : Starting Address of the Register.
00th Command(Read) : Defines the starting address of the 1st half of the register.
01th Command(Read) : Defines the starting address of the 2nd half of the register.
* A8 is set to "Low" or "High" by the 00th or 01th Command.
* L must be set to "Low".
* The device ignores any additional input of address cycles than required.
Figure 1-2. K9F1216X0A (X16) FUNCTIONAL BLOCK DIAGRAM

Figure 2-2. K9F1216X0A (X16) ARRAY ORGANIZATION

NOTE: Column Address : Starting Address of the Register.
* L must be set to "Low".
Product Introduction
The K9F1208X0A is a 528Mbit(553,648,218 bit) memory organized as 131,072 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by two NAND structures, totaling 8,192 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4,096 separately erasable 16K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9F1208X0A.

The K9F1208X0A has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Data is latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 64M byte physical space requires 26 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F1208X0A.

The device provides simultaneous program/erase capability up to four pages/blocks. By dividing the memory array into four 128Mbit separate planes, simultaneous multi-plane operation dramatically increases program/erase performance by 4X while still maintaining the conventional 512 byte(X8 device) or 256 word(X16 device) structure. The extended pass/fail status for multi-plane program/erase allows system software to quickly identify the failing page/block out of selected multiple pages/blocks. Usage of multi-plane operations will be described further throughout this document.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another of the same plane without the need for transporting the data to and from the external buffer memory. Since the time-consuming burst-reading and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

The device includes one block sized OTP(One Time Programmable), which can be used to increase system security or to provide identification capabilities. Detailed information can be obtained by contact with Samsung.

Table 1. Command Sets

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Read 1</td>
<td>00h/01h(1)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Read 2</td>
<td>50h</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Read ID</td>
<td>90h</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Reset</td>
<td>FFh</td>
<td>-</td>
<td>-</td>
<td>O</td>
</tr>
<tr>
<td>Page Program (True)(2)</td>
<td>80h</td>
<td>10h</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Page Program (Dummy)(2)</td>
<td>80h</td>
<td>11h</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Copy-Back Program(True)(2)</td>
<td>00h</td>
<td>8Ah</td>
<td>10h</td>
<td>-</td>
</tr>
<tr>
<td>Copy-Back Program(Dummy)(2)</td>
<td>03h</td>
<td>8Ah</td>
<td>11h</td>
<td>-</td>
</tr>
<tr>
<td>Block Erase</td>
<td>60h</td>
<td>D0h</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Multi-Plane Block Erase</td>
<td>60h------60h</td>
<td>D0h</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Read Status</td>
<td>70h</td>
<td>-</td>
<td>-</td>
<td>O</td>
</tr>
<tr>
<td>Read Multi-Plane Status</td>
<td>71h(3)</td>
<td>-</td>
<td>-</td>
<td>O</td>
</tr>
</tbody>
</table>

**NOTE:** 1. The 00h command defines starting address of the 1st half of registers. The 01h command defines starting address of the 2nd half of registers. After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.

2. Page Program(True) and Copy-Back Program(True) are available on 1 plane operation. Page Program(Dummy) and Copy-Back Program(Dummy) are available on the 2nd,3rd,4th plane of multi plane operation.

3. The 71h command should be used for read status of Multi Plane operation.

**Caution:** Any undefined command inputs are prohibited except for above command set of Table 1.
Memory Map

The device is arranged in four 128Mbit memory planes. Each plane contains 1,024 blocks and 528 byte (X8 device) or 264 word (X16 device) page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that multi-plane program/erase operations can be executed for every four sequential blocks.

Figure 3. Memory Array Map
**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>K9F12XXQ0A(1.8V)</th>
<th>K9F12XXU0A(3.3V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage on any pin relative to VSS</td>
<td>VOUT</td>
<td>-0.6 to +2.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC</td>
<td>-0.2 to +2.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCCQ</td>
<td>-0.2 to +2.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Under Bias</td>
<td>TBIAS</td>
<td>-10 to +125</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSTG</td>
<td>-65 to +150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>Ios</td>
<td>5</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

(Voltage reference to GND, K9F12XXX0A-XCB0 : TA=0 to 70°C, K9F12XXX0A-XIB0: TA=-40 to 85°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>1.70</td>
<td>1.8</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>Vccq</td>
<td>1.70</td>
<td>1.8</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>Vss</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**DC AND OPERATING CHARACTERISTICS**

(Recommended operating conditions otherwise noted.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>K9F12XXQ0A(1.8V)</th>
<th>K9F12XXU0A(3.3V)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Current</td>
<td>iOC1</td>
<td>tRC=50ns, CE=VIL</td>
<td>-</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>iOC2</td>
<td></td>
<td>-</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>iOC3</td>
<td>-</td>
<td>8</td>
<td>15</td>
<td>-</td>
</tr>
<tr>
<td>Stand-by Current(TTL)</td>
<td>iIS1</td>
<td>CE=Vih, WP=0V/Vcc</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Stand-by Current(CMOS)</td>
<td>iIS2</td>
<td>CE=Vcc-0.2, WP=0V/Vcc</td>
<td>-</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>ILI</td>
<td>Vih=0 to Vcc(max)</td>
<td>-</td>
<td>-</td>
<td>±10</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>ILO</td>
<td>VOUT=0 to Vcc(max)</td>
<td>-</td>
<td>-</td>
<td>±10</td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>HIH</td>
<td>I/O pins</td>
<td>Vcc-0.4</td>
<td>-</td>
<td>VccQ+0.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Except I/O pins</td>
<td>Vcc-0.4</td>
<td>-</td>
<td>VccQ+0.3</td>
</tr>
<tr>
<td>Input Low Voltage, All inputs</td>
<td>HIL</td>
<td>-</td>
<td>-0.3</td>
<td>-</td>
<td>0.4</td>
</tr>
<tr>
<td>Output High Voltage Level</td>
<td>HOH</td>
<td>K9F12XXQ0A :KH=+100µA, K9F12XXU0A :KH=+400µA</td>
<td>VccQ-0.1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output Low Voltage Level</td>
<td>HOL</td>
<td>K9F12XXQ0A :KL=+100µA, K9F12XXU0A :KL=+2.1mA</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
</tr>
<tr>
<td>Output Low Current(R@)</td>
<td>I(O/R)</td>
<td>K9F12XXQ0A :VOH=+0.1V, K9F12XXU0A :VOL=+0.4V</td>
<td>3</td>
<td>4</td>
<td>8</td>
</tr>
</tbody>
</table>
VALID BLOCK

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid Block Number</td>
<td>Nvb</td>
<td>4,026</td>
<td>-</td>
<td>4,096</td>
<td>Blocks</td>
</tr>
</tbody>
</table>

NOTE:
1. The K9F12XXA0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for an appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

AC TEST CONDITION
(K9F12XXX0A-XCB0 : TA=0 to 70°C, K9F12XXX0A-XIB0: TA=−40 to 85°C  
K9F12XXQ0A : Vcc=1.70V~1.95V ,  K9F12XXU0A : Vcc=2.7V~3.6V unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>K9F12XXQ0A</th>
<th>K9F12XXU0A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Levels</td>
<td>0V to VccQ</td>
<td>0.4V to 2.4V</td>
</tr>
<tr>
<td>Input Rise and Fall Times</td>
<td>5ns</td>
<td>5ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>VccQ/2</td>
<td>1.5V</td>
</tr>
<tr>
<td>K9F12XXQ0A:Output Load (VccQ:1.8V +/-10%)</td>
<td>1 TTL GATE and CL=30pF</td>
<td>1 TTL GATE and CL=50pF</td>
</tr>
<tr>
<td>K9F12XXU0A:Output Load (VccQ:3.3V +/-10%)</td>
<td>-</td>
<td>1 TTL GATE and CL=100pF</td>
</tr>
</tbody>
</table>

CAPACITANCE (TA=25°C, Vcc=1.8V/3.3V, f=1.0MHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/Output Capacitance</td>
<td>Ci/O</td>
<td>VIL=0V</td>
<td>-</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>CiN</td>
<td>VIN=0V</td>
<td>-</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

<table>
<thead>
<tr>
<th>CLE</th>
<th>ALE</th>
<th>CE</th>
<th>WE</th>
<th>RE</th>
<th>WF</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Read Mode</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Write Mode</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Data Input</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>Data Output</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>0V/Vcc (2)</td>
<td>Stand-by</td>
</tr>
</tbody>
</table>

NOTE: 1. X can be VIL or VIH.
2. WF should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program Time</td>
<td>BPROG</td>
<td>-</td>
<td>200</td>
<td>500</td>
<td>µs</td>
</tr>
<tr>
<td>Dummy Busy Time for Multi Plane Program</td>
<td>DDBSY</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Number of Partial Program Cycles in the Same Page</td>
<td>Main Array</td>
<td>Nop</td>
<td>-</td>
<td>1</td>
<td>cycle</td>
</tr>
<tr>
<td>Number of Partial Program Cycles in the Same Page</td>
<td>Spare Array</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>cycles</td>
</tr>
<tr>
<td>Block Erase Time</td>
<td>BERS</td>
<td>2</td>
<td>3</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>
AC Timing Characteristics for Command / Address / Data Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLE Set-up Time</td>
<td>tCLS</td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CLE Hold Time</td>
<td>tCLH</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CE Setup Time</td>
<td>tCS</td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CE Hold Time</td>
<td>tCH</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>WE Pulse Width</td>
<td>tWP</td>
<td>25 (1)</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Setup Time</td>
<td>tALS</td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>ALE Hold Time</td>
<td>tALH</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>tDS</td>
<td>20</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>tDH</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Write Cycle Time</td>
<td>tWC</td>
<td>45</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>WE High Hold Time</td>
<td>tWH</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE:**
1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Transfer from Cell to Register</td>
<td>tr</td>
<td>-</td>
<td>12</td>
<td>µs</td>
</tr>
<tr>
<td>ALE to RE Delay</td>
<td>tAR</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CLE to RE Delay</td>
<td>tCLR</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Ready to RE Low</td>
<td>tRR</td>
<td>20</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>RE Pulse Width</td>
<td>tRP</td>
<td>25</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>WE High to Busy</td>
<td>tWB</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Read Cycle Time</td>
<td>tRC</td>
<td>50</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>CE Access Time</td>
<td>tCEA</td>
<td>-</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>RE Access Time</td>
<td>tREA</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>RE High to Output Hi-Z</td>
<td>tRHZ</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>CE High to Output Hi-Z</td>
<td>tCHZ</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>RE or CE High to Output hold</td>
<td>tOH</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>RE High Hold Time</td>
<td>tRHE</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Output Hi-Z to RE Low</td>
<td>tIR</td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>WE High to RE Low</td>
<td>tWHR</td>
<td>60</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Device Resetting Time(Read/Program/Erase)</td>
<td>trST</td>
<td>-</td>
<td>5/10/500(1)</td>
<td>µs</td>
</tr>
<tr>
<td>Last RE High to Busy(at sequential read)</td>
<td>trB</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>CE High to Ready(in case of interception by CE at read)</td>
<td>tCRY</td>
<td>-</td>
<td>50 +tr(R/B)(2)</td>
<td>ns</td>
</tr>
<tr>
<td>CE High Hold Time(at the last serial read)(2)</td>
<td>tCEH</td>
<td>100</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE:**
1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, CE must be held high for longer time than ICEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte(X8 device) or 1st word(X16 device) in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh(X8 device) or non-FFFFh(X16 device) data at the column address of 517(X8 device) or 256 and 261(X16 device). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 4). Any intentional erasure of the original invalid block information is prohibited.

Figure 4. Flow chart to create invalid block table.
NAND Flash Technical Notes (Continued)

Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Detection and Countermeasure sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td></td>
</tr>
<tr>
<td>Erase Failure</td>
<td>Status Read after Erase --&gt; Block Replacement</td>
</tr>
<tr>
<td>Program Failure</td>
<td>Status Read after Program --&gt; Block Replacement Read back (Verify after Program) --&gt; Block Replacement or ECC Correction</td>
</tr>
<tr>
<td>Read</td>
<td></td>
</tr>
<tr>
<td>Single Bit Failure</td>
<td>Verify ECC --&gt; ECC Correction</td>
</tr>
</tbody>
</table>

ECC

: Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

![Program Flow Chart Diagram]

If ECC is used, this verification operation is not needed.

- Write 00h
- Write Address
- Wait for tR Time
- Verify Data
- Yes: Program Completed
- No:
  - Program Error
  - If program operation results in an error, map out the block including the page in error and copy the target data to another block.
**NAND Flash Technical Notes** (Continued)

### Erase Flow Chart

1. **Start**
2. Write 60h
3. Write Block Address
4. Write D0h
5. Read Status Register
6. If \(I/O\ 6 = 1\) or \(R/B = 1\), then:
   - If \(I/O\ 0 = 0\), then:
     - Erase Error
   - Erase Completed

### Read Flow Chart

1. **Start**
2. Write 00h
3. Write Address
4. Read Data
5. ECC Generation
6. Verify ECC
7. If ECC is verified, then:
   - Page Read Completed
8. If ECC is not verified, then:
   - Reclaim the Error

\(*\) : If erase operation results in an error, map out the failing block and replace it with another block.

### Block Replacement

**Step1**
When an error happens in the nth page of the Block ‘A’ during erase or program operation.

**Step2**
Copy the nth page data of the Block ‘A’ in the buffer memory to the nth page of another free block (Block ‘B’).

**Step3**
Then, copy the data in the 1st \((n-1)\) th page to the same location of the Block ‘B’.

**Step4**
Do not further erase Block ‘A’ by creating an ‘invalid Block’ table or other appropriate scheme.
Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area (0~255 byte), '01h' command sets the pointer to 'B' area (256~511 byte), and '50h' command sets the pointer to 'C' area (512~527 byte). With these commands, the starting column address can be set to any of a whole page (0~527 byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

### Table 2. Destination of the pointer

<table>
<thead>
<tr>
<th>Command</th>
<th>Pointer position</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>0 ~ 255 byte</td>
<td>1st half array (A)</td>
</tr>
<tr>
<td>01h</td>
<td>256 ~ 511 byte</td>
<td>2nd half array (B)</td>
</tr>
<tr>
<td>50h</td>
<td>512 ~ 527 byte</td>
<td>spare array (C)</td>
</tr>
</tbody>
</table>

- **A** area (00h plane) 256 Byte
- **B** area (01h plane) 256 Byte
- **C** area (50h plane) 16 Byte

**Figure 5. Block Diagram of Pointer Operation**

(1) **Command input sequence for programming 'A' area**

The address pointer is set to 'A' area (0~255), and sustained

```
00h     80h     10h
```

'00h' command can be omitted.

(2) **Command input sequence for programming 'B' area**

The address pointer is set to 'B' area (256~511), and will be reset to 'A' area after every program operation is executed.

```
01h     80h     10h
```

'B', 'C' area can be programmed. It depends on how many data are inputted.

01h command must be rewritten before every program operation

(3) **Command input sequence for programming 'C' area**

The address pointer is set to 'C' area (512~527), and sustained

```
50h     80h     10h
```

Only 'C' area can be programmed.

'50h' command can be omitted.
Samsung NAND Flash has two address pointer commands as a substitute for the most significant column address. '00h' command sets the pointer to 'A' area (0~255 word), and '50h' command sets the pointer to 'B' area (256~263 word). With these commands, the starting column address can be set to any of a whole page (0~263 word). '00h' or '50h' is sustained until another address pointer command is inputted. To program data starting from 'A' or 'B' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary.

### Table 3. Destination of the pointer

<table>
<thead>
<tr>
<th>Command</th>
<th>Pointer position</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>0 ~ 255 word</td>
<td>main array (A)</td>
</tr>
<tr>
<td>50h</td>
<td>256 ~ 263 word</td>
<td>spare array (B)</td>
</tr>
</tbody>
</table>

### Figure 6. Block Diagram of Pointer Operation

(1) Command input sequence for programming 'A' area

The address pointer is set to 'A' area (0~255), and sustained

'00h' command can be omitted.

(2) Command input sequence for programming 'B' area

The address pointer is set to 'B' area (256~263), and sustained

Only 'B' area can be programmed. '50h' command can be omitted.
System Interface Using $\overline{CE}$ don’t t-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528-byte 1264-word page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 7. Program Operation with $\overline{CE}$ don’t t-care.

Figure 8. Read Operation with $\overline{CE}$ don’t t-care.

On K9F1208U0A-Y,P or K9F1208U0A-V,F $\overline{CE}$ must be held low during $t_R$.
<table>
<thead>
<tr>
<th>Device</th>
<th>I/O</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>K9F1208X0A(X8 device)</td>
<td>I/O 0 ~ I/O 7</td>
<td>~528byte</td>
</tr>
<tr>
<td>K9F1216X0A(X16 device)</td>
<td>I/O 0 ~ I/O 15</td>
<td>~264word</td>
</tr>
</tbody>
</table>

**NOTE:**
1. I/O8~15 must be set to “0” during command or address input.
2. I/O8~15 are used only for data bus.

* Command Latch Cycle

* Address Latch Cycle

### SAMSUNG ELECTRONICS
* Input Data Latch Cycle

CLE

\[ T_{CLH} \]

CE

\[ T_{CH} \]

ALE

\[ T_{ALS}, T_{WC} \]

WE

\[ T_{WP}, T_{WH}, T_{DS}, T_{DH}, T_{WC} \]

I/Ox

\[ DIN_0, DIN_1, DIN_n \]

* Serial access Cycle after Read (CLE=L, WE=H, ALE=L)

CE

\[ T_{RC} \]

RE

\[ T_{REA}, T_{REH}, T_{IRHZ}, T_{OH} \]

I/Ox

\[ Dout \]

R/B

\[ T_{IRR} \]

NOTES: Transition is measured ±200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
* Status Read Cycle

**READ1 OPERATION (READ ONE PAGE)**

- **CLE**
- **CE**
- **WE**
- **ALE**
- **RE**
- **I/Ox**
- **R/B**

**NOTES**: 1) is only valid on K9F1208U0A-Y,P or K9F1208U0A-V,F

X8 device : m = 528, Read CMD = 00h or 01h
X16 device : m = 264, Read CMD = 00h

---

**SBM**: YCB0, YIB0, PCB0, PIB0, DCB0, DIB0, HCB0, HIB0
**SBM**: VC0, VIB0, FCB0, FIB0, DC0, DIB0, HCB0, HIB0
Read1 Operation (Intercepted by CE)

CLE

CE

WE

ALE

RE

I/Ox

R/B

Read2 Operation (Read One Page)

CLE

CE

WE

ALE

RE

I/Ox

R/B

M Address:

A0 ~ A3: Valid Address
A4 ~ A7: Don't care

Start address M

SAMSUNG ELECTRONICS
Sequential Row Read Operation (Within a Block)

**CLE**

**CE**

**WE**

**ALE**

**RE**

**I/Ox**

**R/B**

Page Program Operation

**CLE**

**CE**

**WE**

**ALE**

**RE**

**I/Ox**

**R/B**
BLOCK ERASE OPERATION (ERASE ONE BLOCK)

- **CLE**
- **CE**
- **WE**
- **ALE**
- **RE**

**I/Ox**
- 60h: Auto Block Erase Setup Command
- 70h: Read Status Command

**R/B**
- Page (Row) Address
- Busy

**Command I/O**
- 0: Error in Erase
- 0: Successful Erase
- 1: Error in Erase

**TWC**
- **TWB**
- **IBERS**

**A9 ~ A24, A9 ~ A16**

**DCh**

**Page (Row) Address**

**FLASH MEMORY**

26
Multi-Plane Block Erase Operation

* For Multi-Plane Erase operation, Block address to be erased should be repeated before "D0H" command.

Ex.) Four-Plane Block Erase Operation
Read ID Operation

CLE

CE

WE

ALE

RE

I/Ox

90h

00h

ECh

76h

A5h

C0h

Read ID Command

Address, 1 cycle

Maker Code

Device Code

Multi Plane Code

ID Definition Table

90 ID : Access command = 90H

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1\textsuperscript{st} Byte</td>
<td>ECh</td>
</tr>
<tr>
<td>2\textsuperscript{nd} Byte</td>
<td>76h</td>
</tr>
<tr>
<td>3\textsuperscript{rd} Byte</td>
<td>A5h</td>
</tr>
<tr>
<td>4\textsuperscript{th} Byte</td>
<td>C0h</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>K9F1208Q0A</td>
<td>36h</td>
</tr>
<tr>
<td>K9F1208U0A</td>
<td>76h</td>
</tr>
<tr>
<td>K9F1216Q0A</td>
<td>XX46h</td>
</tr>
<tr>
<td>K9F1216U0A</td>
<td>XX56h</td>
</tr>
</tbody>
</table>
Copy-Back Program Operation

On K9F1208U0A-Y,P or K9F1208U0A-V,F CE must be held low during IR

Copy-Back Data
Input Command

I/Ox

Busy

Column Address
Page(Row) Address

Busy

Column Address
Page(Row) Address

00h

A0-A7 A1-A17 A20

A0-A7 A1-A17 A20

A0-A7

A0-A7 A1-A17 A20

I/Ox

Read Status Command

I/Ox=0 Successful Program
I/Ox=1 Error in Program

Successful Program
Error in Program

R/B

On K9F1208U0A-Y,P or K9F1208U0A-V,F CE must be held low during IR
Device Operation

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) or 264 words (x16 device) of data within the selected page are transferred to the data registers in less than 10μs (tR). The system controller can detect the completion of this data transfer (tR) by analyzing the output of R/ B pin. CE must be held low while in busy for K9F12XXU0A-YXB0 or K9F1208U0A-VXB0, while CE is don’t-care with K9F12XXX0A-DXB0. If CE goes high before the device returns to Ready, the random read operation is interrupted and Busy returns to Ready as defined by tCRY. Since the operation was aborted, the serial page read does not output valid data. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data starting from the selected column address up to the last column address.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 512 to 527 bytes (x8 device) or 256 to 263 words (x16 device) may be selectively accessed by writing the Read2 command. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figures 7 to 10 show typical sequence and timings for each read operation.

Sequential Row Read is available only on K9F12XXU0A-Y,P or K9F1208U0A-V,F:

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10μs again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given. Figures 9, 10 show typical sequence and timings for sequential row read operation.
Figure 7. Read1 Operation

NOTE: 1) After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle. 01h command is only available on X8 device (K9F1208X0A).
Figure 8. Read2 Operation

Figure 9. Sequential Row Read1 Operation (only for K9F1208U0A-Y,P and K9F1208U0A-V,F valid within a block)

The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given.
**PAGE PROGRAM**

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528 bytes (x8 device) or 264 words (x16 device), in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes (x8 device) or 264 words (x16 device) of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked (Figure 11). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

**Figure 11. Program & Read Status Operation**
BLOCK ERASE

The Erase operation is done on a block (16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only address A14 to A25 is valid while A9 to A13 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 12 details the sequence.

Figure 12. Block Erase Operation

Multi-Plane Page Program

Multi-Plane Page Program is an extension of Page Program, which is executed for a single plane with 528 byte page registers. Since the device is equipped with four memory planes, activating the four sets of 528 byte page registers enables a simultaneous programming of four pages. Partial activation of four planes is also permitted.

After writing the first set of data up to 528 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program (10h) is inputted to finish data-loading of the current plane and move to the next plane. Since no programming process is involved, R/B remains in Busy state for a short period of time (tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit (I/O 6). Then the next set of data for one of the other planes is inputted with the same command and address sequences. After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes. The extended status bits (I/O 1 through I/O 4) are checked by inputting the Read Multi-Plane Status Register. Status bit of I/O 0 is set to “1” when any of the pages fails.

Multi-plane Page Program with “01h” pointer is not supported, thus prohibited.

Figure 13. Four-Plane Page Program
Restriction in addressing with Multi Plane Page Program

While any block in each plane may be addressable for Multi-Plane Page Program, the five least significant addresses (A9-A13) for the selected pages at one operation must be the same. Figure 14 shows an example where 2nd page of each addressed block is selected for four planes. However, any arbitrary sequence is allowed in addressing multiple planes as shown in Figure 15.

Figure 14. Multi-Plane Program & Read Status Operation

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Figure 15. Addressing Multiple Planes

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Figure 16. Multi-Plane Page Program & Read Status Operation

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Multi-Plane Block Erase

Basic concept of Multi-Plane Block Erase operation is identical to that of Multi-Plane Page Program. Up to four blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command followed by three address cycles) may be repeated up to four times for erasing up to four blocks. Only one block should be selected from each plane. The Erase Confirm command initiates the actual erasing process. The completion is detected by analyzing R/B pin or Ready/Busy status (I/O 6). Upon the erase completion, pass/fail status of each block is examined by reading extended pass/fail status (I/O 1 through I/O 4).

Figure 17. Four Block Erase Operation
Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without utilizing an external memory. Since the time-consuming sequently-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal page registers. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A14 and A15 must be the same between source and target page.

Figure 18 shows the command sequence for single plane operation. "When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 18. One Page Copy-Back program Operation
Multi-Plane Copy-Back Program

Multi-Plane Copy-Back Program is an extension of one page Copy-Back Program into four plane operation. Since the device is equipped with four memory planes, activating the four sets of 528 bytes (x8 device) or 264 words (x16 device) page registers enables a simultaneous Multi-Plane Copy-Back programming of four pages. Partial activation of four planes is also permitted.

First, normal read operation with the "00h" command and address of the source page moves the whole 528 byte data into internal page buffers. Any further read operation for transferring the addressed pages to the corresponding page register must be executed with "03h" command instead of "00h" command. Any plane may be selected without regard to "00h" or "03h". Up to four planes may be addressed. Data moved into the internal page registers are loaded into the destination plane addresses. After the input of command sequences for reading the source pages, the same procedure as Multi-Plane Page programming except for a replacement address command with "8Ah" is executed. Since no programming process is involved during data loading at the destination plane address, \( \text{R/B} \) remains in Busy state for a short period of time (tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit (I/O 6). After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes. No pointer operation is supported with Multi-Plane Copy-Back Program. Once the Multi-Plane Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase once the Multi-Plane Copy-Back Program is finished.

Figure 19. Four-Plane Copy-Back Program

![Four-Plane Copy-Back Program Diagram]

Max Three Times Repeatable
Fig 20. Four-Plane Copy-Back Page Program (Continued)
READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

For Read Status of Multi Plane Program/Erase, the Read Multi-Plane Status command (71h) should be used to find out whether multi-plane program or erase operation is completed, and whether the program or erase operation is completed successfully. The pass/fail status data must be checked only in the Ready condition after the completion of Multi-Plane program or erase operation.

Table 4. Read Status Register Definition

<table>
<thead>
<tr>
<th>I/O No.</th>
<th>Status</th>
<th>Definition by 70h Command</th>
<th>Definition by 71h Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O 0</td>
<td>Total Pass/Fail</td>
<td>Pass : &quot;0&quot;</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pass : &quot;0&quot;*1</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 1</td>
<td>Plane 0 Pass/Fail</td>
<td>Must be don’t -cared</td>
<td>Pass : &quot;0&quot;*2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pass : &quot;0&quot;*2</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 2</td>
<td>Plane 1 Pass/Fail</td>
<td>Must be don’t -cared</td>
<td>Pass : &quot;0&quot;*2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pass : &quot;0&quot;*2</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 3</td>
<td>Plane 2 Pass/Fail</td>
<td>Must be don’t -cared</td>
<td>Pass : &quot;0&quot;*2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pass : &quot;0&quot;*2</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 4</td>
<td>Plane 3 Pass/Fail</td>
<td>Must be don’t -cared</td>
<td>Pass : &quot;0&quot;*2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pass : &quot;0&quot;*2</td>
<td>Fail : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 5</td>
<td>Reserved</td>
<td>Must be don’t -cared</td>
<td>Must be don’t -cared</td>
</tr>
<tr>
<td>I/O 6</td>
<td>Device Operation</td>
<td>Busy : &quot;0&quot;</td>
<td>Ready : &quot;1&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Busy : &quot;0&quot;</td>
<td>Ready : &quot;1&quot;</td>
</tr>
<tr>
<td>I/O 7</td>
<td>Write Protect</td>
<td>Protected : &quot;0&quot;</td>
<td>Not Protected : &quot;1&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Protected : &quot;0&quot;</td>
<td>Not Protected : &quot;1&quot;</td>
</tr>
</tbody>
</table>

NOTE: 1. I/O 0 describes combined Pass/Fail condition for all planes. If any of the selected multiple pages/blocks fails in Program/Erase operation, it sets "Fail" flag.
2. The pass/fail status applies only to the corresponding plane.
Read ID
The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacture code (ECh), and the device code (76h), Reserved (A5h), Multi plane operation code (C0h) respectively. A5h must be don’t-cared. C0h means that device supports Multi Plane operation. The command register remains in Read ID mode until further commands are issued to it. Figure 21 shows the operation sequence.

Figure 21. Read ID Operation 1

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>K9F1208Q0A</td>
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<td>XX46h</td>
</tr>
<tr>
<td>K9F1216U0A</td>
<td>XX56h</td>
</tr>
</tbody>
</table>
RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 22 below.

Figure 22. RESET Operation

<table>
<thead>
<tr>
<th>R/B</th>
<th>FFh</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O0–7</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. Device Status

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>After Power-up</th>
<th>After Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read 1</td>
<td></td>
<td>Waiting for next command</td>
</tr>
</tbody>
</table>
The device has a R/ B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/ B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/ B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/ B) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 23). Its value can be determined by the following guidance.

Fig 23 Rp vs tr ,tf & Rp vs ibusy

@ Vcc = 1.8V, Ta = 25°C , C<sub>L</sub> = 30pF

@ Vcc = 3.3V, Ta = 25°C , C<sub>L</sub> = 100pF

Rp value guidance

Rp(min, 1.8V part) = \( \frac{V_{CC\text{Max}} - V_{OL\text{Max}}}{I_{OL} + \sum I_{L}} \) = 1.85V

Rp(min, 3.3V part) = \( \frac{V_{CC\text{Max}} - V_{OL\text{Max}}}{I_{OL} + \sum I_{L}} \) = 3.2V

where IL is the sum of the input currents of all devices tied to the R/ B pin.

Rp(max) is determined by maximum permissible limit of tr
Data Protection & Power-up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V (1.8V device) or 2V (3.3V device). WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10 µs is required before internal circuit gets ready for any command sequences as shown in Figure 24. The two step command sequence for program/erase provides additional software protection.

Figure 24. AC Waveforms for Power Transition