130nm Flash+Logic: Technology and Applications

Wireless Internet on a Chip – Enabled by Silicon Integration

Al Fazio
Intel Corporation
Outline

- Motivation for Flash + Logic Integration
- Technology Challenges
- Meeting The Challenges
- Product Applications
- Conclusions
Outline

- Motivation for Flash + Logic Integration
- Technology Challenges
- Meeting The Challenges
- Product Applications
- Conclusions
“Wireless Internet on a Chip”

Vision: Cellular Silicon Function Integration for Cost, Performance, Power, and Size

Major “Silicon” Components of a Cellular System

- Digital/Analog
  - Applications Processor
  - Digital Signal Processor
  - Baseband Logic
  - Peripherals
  - SRAM Memory
  - Flash Memory

- RF/Analog
  - Radio Transmit
  - Radio Receive
  - Radio Power Amp
  - Radio Passives
  - Power Supplies

- Intel® Micro Signal Architecture
  - Baseband Processor
  - RF Transceiver
  - Analog Mixed Signal
  - Power Management

- Intel® XScale™ Processor
- Internal SRAM
- Additional Intel® Flash & SRAM as Needed

What is the Optimal Integration Strategy?
Factors Determining Function Partitioning:
- Technology Capability & Cost Optimization
- Board Space (I/O) & Cost Minimization
- Power/Performance Optimization
- Noise Isolation
Technologies for Integration

First Steps – Integrate Digital and Memory Subsystems

Values:
- High Performance of Wide Internal Bus
- Low Power/Noise with No External Bus
- Small Form Factor with Fewer I/O’s

Synergies:
- Moore’s Law Scaling (2x/2yr)
- Synergistic Si Technologies
- Mature, Volume Technologies
Integration: Power-Performance Improvements

Internal vs. External Memory Power Consumption

(CPUs normalized to 312 MHz)

Integrated Flash

<1V Core
<1v I/O

Internal Priority Code Flash

External Embedded Memory

1.8v Core
1.8-1.5v I/O

SDRAM Memory

3v > 1.8v Core
1.8v I/O

Card Memory

3v Core
3v I/O

Lower Memory Latencies through Integration

Increasing Battery Life

Power mW

Increasing Performance

Intel Proc w/ Int Flash

Others

Intel Gen Apps

80/20 int/ext mem split

Integrated Only

Integrated Flash

<1V Core
<1v I/O

Internal Priority Code Flash

External Embedded Memory

1.8v Core
1.8-1.5v I/O

SDRAM Memory

3v > 1.8v Core
1.8v I/O

Card Memory

3v Core
3v I/O

Lower Memory Latencies through Integration

Increasing Battery Life

Power mW

Increasing Performance

Intel Proc w/ Int Flash

Others

Intel Gen Apps

80/20 int/ext mem split

Integrated Only

Integrated Flash

<1V Core
<1v I/O

Internal Priority Code Flash

External Embedded Memory

1.8v Core
1.8-1.5v I/O

SDRAM Memory

3v > 1.8v Core
1.8v I/O

Card Memory

3v Core
3v I/O

Lower Memory Latencies through Integration
Outline

- Motivation for Flash + Logic Integration
- Technology Challenges
- Meeting The Challenges
- Product Applications
- Conclusions
Key Challenges for Integration:

- **Small & Identical** memory cell size integrated vs. discrete
  - Same cell size: Integration (SOC) & Stacking (SIP) Complementary

- **Multiple Gate Oxides**
  - Advanced Logic Gates, Advanced Memory Gates & Support Gates

- **Low Thermal Budget**
  - Advanced Logic Transistors

- **Trench Isolation & Salicide Integration**
  - Small SRAM cell size, Advanced Logic Transistors

- **Multi-Layer Metal**
  - High Gate Density

- **Cost Effective Integration**
  - Minimize flash or logic unique high cost process steps
Outline

- Motivation for Flash + Logic Integration
- Technology Challenges
- Meeting The Challenges
- Product Applications
- Conclusions
Small & Identical memory cell size integrated vs. discrete

“Manitoba”

0.16μ² Flash
# Multiple Gate Oxides

<table>
<thead>
<tr>
<th></th>
<th>Discrete Flash</th>
<th>Integrated Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tunnel Oxide</td>
<td>9nm</td>
<td>9nm</td>
</tr>
<tr>
<td>High Voltage</td>
<td>15nm</td>
<td>15nm</td>
</tr>
<tr>
<td>I/O</td>
<td>7nm</td>
<td>7nm</td>
</tr>
<tr>
<td>High Performance Logic</td>
<td>NA</td>
<td>2.4nm</td>
</tr>
</tbody>
</table>

**One Additional Gate Oxide:**

Evolution of base Flash Process
Low Thermal Budget

- Flash Cell formed prior to Logic Gate
- Basic Process Flow:
  - Flash Tunnel Oxide
  - Flash Floating Gate Poly
  - Flash ONO
  - Flash High Voltage Oxide
  - I/O Oxide
  - Logic Oxide
  - Flash and Logic Gate Patterning
  - S/D Implants

Standard Flash Flow

Standard Logic Flow

Flash+Logic Flow
Trench Isolation & Salicide

- Source
- Drain
- Poly-1
- Poly-2
- Spacer
- Salicide
High Density/ High Performance: 110nm Poly Gate for Logic Performance

SRAM Cell
6 Layer Metal for Logic Density

6 Metal Stack  Al Metal & W plug Via

6 Metal Architecture, Low K Dielectric
Wireless Internet on a Chip – Enabled by Silicon Integration

“Manitoba”

State of the Art: Flash + SRAM + Logic
= Leadership Integration
= High Performance + Low Power + Small Size
Cost Effective Integration

- Only 1 critical mask required over logic (flash gate)
  - Lab feasibility demonstrating ability to share with logic gate
- Other steps are shared (isolation, contact...), non-critical layers (implants...), or self-aligned
Key Attributes for Integration: 
ETOX® Flash Meets All Criteria

- **Small & Identical cell size integrated vs. discrete**
  - Flash: $<10\lambda^2$ cell size, $<5\lambda^2$ with MLC
  - Same cell size: Integration (SOC) & Stacking (SIP) Complementary

- **Multiple Gate Oxides**
  - Discrete Flash processing includes multiple gates

- **Low Thermal Budget**
  - Flash cell processing precedes logic gate formation

- **Trench Isolation & Salicide Integration**
  - Discrete Flash integrates trench & salicide since 0.25$\mu$m node

- **Multi-Layer Metal**
  - Flash & Logic fully compatible

- **Cost Effective Integration**
  - Only 1 additional critical mask required over logic (flash gate)
    - Lab feasibility demonstrating ability to share this layer with logic gate
  - Other steps are shared (isolation, contact...), non-critical layers
    - Intel (implants...), or self-aligned
Outline

- Motivation for Flash + Logic Integration
- Technology Challenges
- Meeting The Challenges
- Product Applications
- Conclusions
Intel® PXA800F Cellular Processor

- Intel® 0.13µ Flash + Logic Process Technology
  - First to market with F+L process for communications

- Intel® XScale™ microarchitecture
  - 104MHz & 312MHz Operating Freq. with 4MB Integrated Intel® OnChip Flash and 512kB SRAM
  - Provides high performance levels for mainstream phones

- Intel® Micro Signal Architecture
  - 104MHz Max Operating Freq. with 512kB Integrated Intel® OnChip Flash Memory and 64kB SRAM

- Integrated Power Management and Peripherals
  - Integrated USB, SD/MMC/MS, LCD, IRDA, BlueTooth* I/F, Camera I/F and other key peripherals reduce need for separate ICs
  - More power management capabilities than previous Intel® XScale™ technology–based products

*Other Names and Brands may be claimed as the property of others.
Intel® PXA800F Cellular Processor Performance Headroom

- **Applications Headroom**
  - Intel® XScale™ core runs all applications
  - At 312MHz for enhanced applications capabilities than today’s GSM/GPRS solutions

- **Communications Headroom**
  - Continuous GPRS Data (Class B)
  - Intel® MSA is running L1 & Intel® XScale™ core is running L2 and L3
  - Estimates for L2/L3 = 14MIPS

*All estimates are provided for planning purposes only and are subject to change without notice

*Other Names and Brands may be claimed as the property of others.*
Intel® PXA800F Cellular Processor
Space Savings

GSM/GPRS Baseband

External Memory Configuration

>200MHz Applications Processor

Apps CPU (17x17)

32Mb Flash (7.7x9)

4Mb SRAM (6x7)

32Mb Flash

GSM/GPRS Baseband (12x12)

PXA800F (312MHz) (12x12)

One Third
The Board Space
Vs 4-5 Discrete

Save Space
and/or
Reduce Board Size

(Package Sizes proportionally correct)
Full GSM/GPRS System Solution

- L1 protocol software available from Intel
- L2/L3 protocol software available from TTPCOM*
  - Physical layer firmware
  - Baseline MMI
  - Full featured API for customer application development
- Industry-proven mixed signal and NZIF/DDC RF solution
- Optimized Power Management Solution from Dialog*
- Handset Reference from Elektrobit* design targeted for availability in Q2’03**
Leadership By Integration

Computing + Communications on One Chip

Silicon Level Integration
- Functions combined on single chip

Package Level Integration
- Stacked discrete chips and packages

Functions on Discrete Chips
- Flash, Applications processors, Cellular chipsets

2002 2004 2006
Conclusions

● A “Wireless Internet on a Chip Technology, Flash + Logic Integration, has been cost effectively achieved without compromising either flash density or logic performance.

● Enables higher performance, lower power and smaller form factor.

● Provides communication, compute and memory functions on a single chip required to drive the next generation of cell phones.