IT-SRAM®: The Memory for SOC

Mark-Eric Jones
MoSys, Inc.
Driving memory innovation

- Founded in 1991 to develop leading-edge memory products based on a novel RAM architecture
  - MDRAM® products introduced in 1995
  - 1T-SRAM® standard SRAM-function products since 1998

- Un-matched memory technology development team
  - Headquartered in Sunnyvale, California
  - 90 employees
  - 40 US patents granted
  - Many additional patents pending

- Recognized with industry-leading awards
  - Top 25 Digital ICs: Cahners Electrical Group 1999
  - Most Innovative Memory: Semiconductor Insights 2000, 2002

- IPO June 28, 2001 NASDAQ symbol “MOSY”
Key business milestones

- **March 1999**
  - MoSys starts licensing of 1T-SRAM® technology

- **August 2000**
  - First MoSys licensee starts 1T-SRAM® SoC production

- **June 2001**
  - MoSys completes IPO on NASDAQ (Ticker: “MOSY”)

- **September 2001**
  - IP licensing becomes majority of MoSys’ revenue

- **May 2002**
  - Dataquest confirms MoSys fastest IP growth*

* Worldwide IP revenue & royalty growth of top 20 IP revenue companies
SoC memory continues to increase

SoC memory content continues to grow as % of silicon area

Source: SIA ITRS
Existing Solutions

Random Access Speed

Density

Embedded DRAM

6T SRAM
1T-SRAM®: Performance with lowest cost
1T-SRAM® size comparison

6 transistor SRAM storage cell

1T-SRAM storage cell

50-70% less silicon area

Over 70% less cost
SoC memory cost

Mbit/$ vs Feature Size (micron)

- 1T-SRAM
- 6T SRAM
1T-SRAM process life cycle

- 1999: 0.25 µm
- 2000: 0.22 µm
- 2001: 0.18 µm
- 2002: 0.15 µm
- 2003: 0.13 µm
- 2004: 0.09 µm
## 1T-SRAM® scalability

<table>
<thead>
<tr>
<th></th>
<th>0.25µm</th>
<th>0.22µm</th>
<th>0.18µm</th>
<th>0.15µm</th>
<th>0.13µm</th>
<th>0.09µm</th>
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<tbody>
<tr>
<td><strong>1T-SRAM®</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bitcell (µm²)</td>
<td>3.51</td>
<td>2.72</td>
<td>1.97</td>
<td>1.46</td>
<td>1.10</td>
<td>0.61</td>
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<tr>
<td>Macro (mm²/Mbit)</td>
<td>7.0</td>
<td>5.0</td>
<td>3.6</td>
<td>2.6</td>
<td>1.9</td>
<td>1.1</td>
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<tr>
<td><strong>6T SRAM</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bitcell (µm²)</td>
<td>7.56</td>
<td>5.85</td>
<td>4.65</td>
<td>3.42</td>
<td>2.43</td>
<td>1.36</td>
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<tr>
<td>Macro (mm²/Mbit)</td>
<td>11.28</td>
<td>8.74</td>
<td>7.18</td>
<td>5.02</td>
<td>3.73</td>
<td>2.09</td>
</tr>
</tbody>
</table>
Memory Technology Quality
IP challenges

- Digital IP
  - Design challenge is functional correctness

- Memory & Analog IP
  - Design challenge is yield and manufacturability
Quality

Achievement of desired results:

- During manufacture
  - Yield
- After manufacture
  - Reliability
- During use
  - Soft Error Rate
Yield models for 0.13µ SRAM

![Graph showing yield models for 0.13µ SRAM]
Reliability qualification

- Joint MoSys-TSMC 1T-SRAM® reliability programs
  - Qualification in 0.25µ, 0.18µ, 0.13µ completed
  - 1000 Hours HTOL passed
  - SER passed
Soft error rate (SER)

- Mis-operation due to alpha particles or cosmic rays affects DRAM and today especially SRAM
- Even CMOS latches will be affected in UDSM processes
- Failures measured in FITs (failure in billion device hours)
- 1000 FITs will translate to device MTBF of 114 years
Soft error mechanism

Particle generates cloud of Hole-Electron pairs as it passes through the Silicon

Alpha Particle or Cosmic Ray

Silicon
System implications of SER

What are the system effects of SER?

Illegal operation program must terminate

Close
Effect depends on application
Failure rate

Mean time to failure of systems depends on:

- Memory soft error rate (FITs/Mbit)
- Amount of memory in each system (Mbits)
- System susceptibility to memory errors
- Number of systems

\[
\text{MTTF} = \frac{1}{(\text{SER}) \times (\text{Memory Size}) \times (\text{System Susceptibility}) \times (\# \text{ of Systems})}
\]
SRAM soft error rates

![Graph showing SRAM soft error rates across different process generations. The graph plots FITs/Mb (200MHz) on the y-axis and Process Generation on the x-axis. The graph shows three different types of SRAM: 1T-SRAM, Pseudo-6T, and 6T-SRAM. Each type is represented by a different color marker. The y-axis ranges from 1 FIT to 10,000,000 FITs with labels at 10, 100, 1,000, 10,000, 100,000, and 1,000,000. The x-axis ranges from 0.25µm to 0.13µm with labels at 0.25µ, 0.18µ, 0.15µ, and 0.13µ. The graph indicates that as the process generation decreases, the soft error rate increases. Source: MoSys]
1T-SRAM-M™

- Lowest power memory for mobile applications
  - MultiBank® 1T-SRAM® technology
    - Active power as low as ¼ of 6T SRAM due to reduced dimensions and small bank size
  - Avoids 6T SRAM bit cell leakage problem
    - Standby power down to ~10µA/Mbit with data retention (0.13µ logic process)
    - Even lower power deep sleep mode
    - Uses standard logic processes
Bit cell leakage

6 transistor SRAM storage cell

1T-SRAM storage cell

Four Leakage Paths across Supply

One Internal Leakage Path
1T-SRAM-R™

- Built on a Proven 1T-SRAM Foundation
- **Transparent Error Correction™** technology
  - Simplified production flow reduces cost
    - Eliminates Laser Repair Step
  - Dynamic repair enhances reliability
  - Dramatically reduced SER
    - Under 10 FITs/Mbit
- → Without memory silicon area penalty!
1T-SRAM-R™ soft error rate

FITs/Mb (200MHz)

Process Generation

Source: MoSys
Embedded memory reliability

- 1T-SRAM-R
- 6T with Repair + ECC
- 6T with Self Test And Repair
- 6T with Repair
- 6T SRAM no Repair

Life

Power-up

Manufacture
# Embedded Memory Technologies

<table>
<thead>
<tr>
<th></th>
<th>6T SRAM</th>
<th>6T SRAM + repair</th>
<th>6T SRAM + self test and repair</th>
<th>6T SRAM + self test and repair + ECC</th>
<th>1T-SRAM-R</th>
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<tbody>
<tr>
<td><strong>Repair of manufacturing defects?</strong></td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td><strong>Repair of infant mortality defects?</strong></td>
<td>No</td>
<td>No</td>
<td>Limited</td>
<td>Yes</td>
<td>Yes</td>
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<td><strong>Repair of intermittent defects?</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td><strong>Macro area (0.13-micron, mm²/Mbit)</strong></td>
<td>3.8</td>
<td>4.0</td>
<td>4.2</td>
<td>5.2</td>
<td>2</td>
</tr>
<tr>
<td><strong>SER (0.13-micron, 200MHz, FIT/Mbit)</strong></td>
<td>&gt;10,000</td>
<td>&gt;10,000</td>
<td>&gt;10,000</td>
<td>&lt; 10</td>
<td>&lt; 10</td>
</tr>
</tbody>
</table>
1T-SRAM-R™ summary

- Simpler production flow & improved yields lower costs
  - Eliminates laser repair

- Enhanced reliability
  - TEC corrects failures after manufacture

- Dramatically Reduced SER
  - < 10 FIT/Mbit in 0.13-micron

- Without memory silicon area penalty
  - MoSys patented Transparent Error Correction™
Announced licensees

Over 40 Licensed designs delivered.

Over 40 M Licensed chips shipped.

Over 1,000,000,000 Megabits.

+ Newly announced:
  Hudson Soft
  Motorola
  National Semiconductor
  Switchcore
1T-SRAM®: Driving memory integration

- Highest yield, manufacturability and testability
- Lowest SoC cost structure
- Uses standard logic processes
- Lower power consumption than six transistor SRAM
- Simple SRAM interface for ease of design & high speed
- Over 40 customer designs delivered
- Over 40 million SoC chips shipped by customers
1T-SRAM® - The Memory for SoC

END