DDR II - The Evolution Continues
JEDEC Future Dram Task Group

Joe Macri
ATI Technologies
macri@ati.com
408-572-6032
What is the JEDEC Future Dram Task Group?

Established: 4/1998 by JEDEC JC-42 Memory Committee

Scope: Define and develop a long term roadmap detailing the logical, physical and electrical interfaces of future Drams and DIMMs.

Participation: Over 50 companies with expertise in the following:

- Dram manufacturing
- Dimm manufacturing
- PC chipset design
- Microprocessor design
- Server/mainframe/super computer design
- Communications
- Graphics
- Consumer electronics
- Packaging
- Connectors/interconnect
- Support chips
- Modeling
- Test Equipment

Current Task: Develop DDR II Dram and aid the JEDEC committees during the standardization process. The JEDEC committees make the standards, not the task group.

Methods: Bring together a diverse group of companies and engineers

- Everyone, including non-JEDEC members, are welcome to join
- Open forum for sharing new and old concepts
- Education of the group though the guest speakers

Goals: Open standard - Its FREE!

- Low system cost
- Ease of Manufacturability
- High volume
The DDR II Design Philosophy

- Evolution NOT Revolution

- The system is more important than the Dram
- Low cost
- Low power
- Simplify Dram
- Parallel control architecture offers lowest inherent latency
- DDR I backwards compatibility
- Improve bus utilization - More efficient Dram
- No custom Dram interface required on memory controller
  - Compatible with industry standard place/route tools
  - User flexibility
- Invent only what is necessary - Borrow from Srams, SLDram, etc.

Note: This chart is conceptual in nature and should not be used to determine the relative performance differences between devices.
What is DDR II?

- DDR I Backwards Compatibility
- Performance/Bandwidth Improvements
- Cost Improvements
- Power Reduction Improvements
- I/O, Package and Clocking
DDR I Backwards compatibility

- Command set is a super set of DDR I commands
  - DDR II command set can control DDR I

- Basic device timing is the same as DDR I
  - Command bus centered relative to clock
  - Data bus centered relative to strobe on writes
  - Data bus edge aligned to strobe on reads

- 4 Banks

- Page size is the same as DDR I

- I/O structure allows for one controller to communicate to either DDR I or DDR II

- Common DDR I and DDR II DIMM being developed
  - Eases pinout of memory controller
  - 232 pin DIMM

- DDR I compatible Data Mask Support
Performance/Bandwidth Improvements

- Improved I/O structure
  - Mult-drop memory configurations: 400 Mbits/sec/pin
  - 64 bit memory system - 3.2 GBytes/sec
  - Point to point memory configurations: 800 Mbits/sec/pin
  - 64 bit memory system - 6.4 GBytes/sec

- Dram core utilizes a prefetch of 4
  - Decreases frequency of dram core relative needed to support increased data rate
    - Dram core runs at 1/4 data bus frequency

- Commands can be valid on any rising edge of clock
  - Preserves command bus utilization
    - Dram command bus runs at 1/2 data bus frequency

- Posted CAS
  - Increases command bus utilization

- Write latency equals read latency minus one
  - Increases data bus utilization

- Low latency enhancements
  - Exploring Virtual Channel
  - Exploring ESDRAM Lite
Dram Core Data Prefetch Size

Possible choices: 2, 4 or 8

Survey results from Dram vendors on CAS cycle time
Assumptions: ~2002-2003 time frame
256mbit device
Achieve high yield for x4, x8, x16 devices

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Cycle Time</th>
<th>Max pin frequency prefetch 2</th>
<th>Max pin frequency prefetch 4</th>
<th>Max pin frequency prefetch 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7.5ns</td>
<td>266 mbit/sec</td>
<td>533 mbit/sec</td>
<td>1066 mbit/sec</td>
</tr>
<tr>
<td>B</td>
<td>6.6ns</td>
<td>303 mbit/sec</td>
<td>606 mbit/sec</td>
<td>1212 mbit/sec</td>
</tr>
<tr>
<td>C</td>
<td>6.0ns</td>
<td>333 mbit/sec</td>
<td>666 mbit/sec</td>
<td>1333 mbit/sec</td>
</tr>
<tr>
<td>D</td>
<td>6.7ns</td>
<td>298 mbit/sec</td>
<td>597 mbit/sec</td>
<td>1194 mbit/sec</td>
</tr>
<tr>
<td>E</td>
<td>6.5ns</td>
<td>308 mbit/sec</td>
<td>615 mbit/sec</td>
<td>1230 mbit/sec</td>
</tr>
<tr>
<td>F</td>
<td>6.5ns</td>
<td>308 mbit/sec</td>
<td>615 mbit/sec</td>
<td>1230 mbit/sec</td>
</tr>
<tr>
<td>G</td>
<td>6.5ns</td>
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</tr>
</tbody>
</table>

Conclusion: Prefetch 4 core
DDR II Commands/Address - 4n-Rule for Data

- Commands can be issued on any rising edge of clock as long as they do not cause a data bus conflict or interrupt a previous command
- 4 data bus cycles are consumed for all reads and writes

Example 1: CAS Reads to one Dram Bank

Example 2: RAS to one Dram followed by CAS Reads to different Drams
Read and Write Conflicts

Classic Resource Conflict

Write
Read
Transmit Address
Access Array
Transmit Data

Write Conflict

CAS = 2

Address/Control
Data
Array

Read Conflict

CAS = 2

Address/Control
Data
Array

Conclusion: Delayed writes too complicated to implement

Conclusion: Matching write to read latency is simple and will be implemented
Cost Improvements

• Dram core is a prefetch of 4
  • Improves yield at DDR II’s high frequency data rate

• Elimination of interrupt commands
  • Reduces test costs
  • Increases yield due to elimination of speed critical path

• Burst 4 only
  • Reduce test costs

• Elimination of 1/2 cycle latencies
  • Reduces test costs

• Device and DIMM Pinout optimized for low cost motherboard and DIMM routing

• No required custom Dram interface on memory controller
  • Speeds development time
  • Reduces development costs
Burst Length

Possible choices: 2, 4 or 8

Survey results from Dram users

<table>
<thead>
<tr>
<th>User</th>
<th>Burst Length Desired</th>
</tr>
</thead>
<tbody>
<tr>
<td>Server</td>
<td>2 and 4</td>
</tr>
<tr>
<td>A</td>
<td>2, 4 and 8</td>
</tr>
<tr>
<td>B</td>
<td>2, 4 and 8</td>
</tr>
<tr>
<td>C</td>
<td>2, 4 and 8</td>
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</tr>
<tr>
<td>E</td>
<td>2, 4 and 8</td>
</tr>
<tr>
<td><strong>Graphics</strong></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>2, 4 and 8</td>
</tr>
<tr>
<td>G</td>
<td>2 and 4</td>
</tr>
<tr>
<td>H</td>
<td>2 and 4</td>
</tr>
<tr>
<td><strong>Consumer</strong></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>2 and 4</td>
</tr>
<tr>
<td><strong>Module</strong></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>2, 4 and 8</td>
</tr>
</tbody>
</table>

* Since the Dram has a prefetch of 4 core burst length 2 makes no sense

Conclusion: Burst 4 only
Power reduction Improvements

- Dram core is a prefetch of 4
  - Lower core power

- 1.8v Vdd for I/O
  - Lower I/O Power
I/O, Clocking and Package

- **I/O**
  - 1.8v VDDQ
  - SSTL-2 Style of termination
  - Output driver calibration - Under consideration
    - Balanced P/N calibration
    - Absolute Voh/Vol calibration
  - Data Timing calibration - Under consideration
    - Read data calibration support in Dram - 3 Options
      - Dram array (Overwrite array contents)
      - Dedicated read test pattern
      - Write/Read buffer to hold read test pattern
    - Write Data calibration support in Dram
      - Write/Read buffer to hold write test pattern
      - Dram array (Overwrite array contents)
- **Clocking**
  - Differential Strobes - Under consideration
- **FPBGA Package**
  - x4 and x8 package very close to completion
  - x16 and x32 package in development
Where is DDR II in the Standards Process?

The Standards Process

Device and System Definition

System Implementation

Ballot Process

Standard

Build System

Dram Manufacturers
Dram Users

DDR II is in the ballot process

JEDEC Committees

Task Group

Dram Manufacturers
Dram Users

Who To Contact For Information
JEDEC:
Ken McGhee
JEDEC
703-907-7500
kenm@eia.org

Future Dram Task Group:
Joe Macri, Chairman JEDEC’s JC42.3 Dram Committee and Future Dram TG
ATI Technologies
408-572-6032
macri@ati.com

Paul Coteus, Vice Chairman Future Dram Task Group
IBM
coteus@us.ibm.com
914-945-2667