Simplescalar

- What is it?
- Where do I get it?
- How do I run it?
- What can I do with it, and what does it have anything to do with DRAM memory systems?
What is it?

- Simulator written in C
- Tool you can use to “prove” that “machine A” is better than “machine B” without actually building machine A or machine B
- See www.simplescalar.com for more details
Where do I get it?

- www.simplescalar.com
- local version (in beta)
How do I run it?

- See Simplescalar manual
- See UMD DRAM Enhancement manual
What do I do with it, and . . .

- Simplescalar models a virtual computer system, CPU and DRAM memory system inclusive.
- We implemented a basic transaction based memory system for Simplescalar
- Currently Models SDRAM/DDR SDRAM and DRDRAM.
- You can use it to model “Your memory system”, and show IPC improvements
Looks Familiar

Execution of a Load Instruction in an Abstract Modern Processor

** Steps not required for some processor/system controllers. Protocol dependant.
Simulated BIU

Bus Interface in Simulated CPU

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Bus Interface Data Structure
Simulated Memory Controller

Transaction Queue and Memory Controller(s) Structure
Suggestions

- Download Simplescalar simulator
- Download some workloads (benchmarks)
- look at sample commands, modify for your own use
- Compile for use with Alpha binaries
- Obtain some IPC numbers to gain familiarity
- Try to understand how simulator models SDRAM/DDR SDRAM memory systems
- Create new DRAM type, modify SDRAM/DDR SDRAM models to match your model.
- Simulate. Report Results